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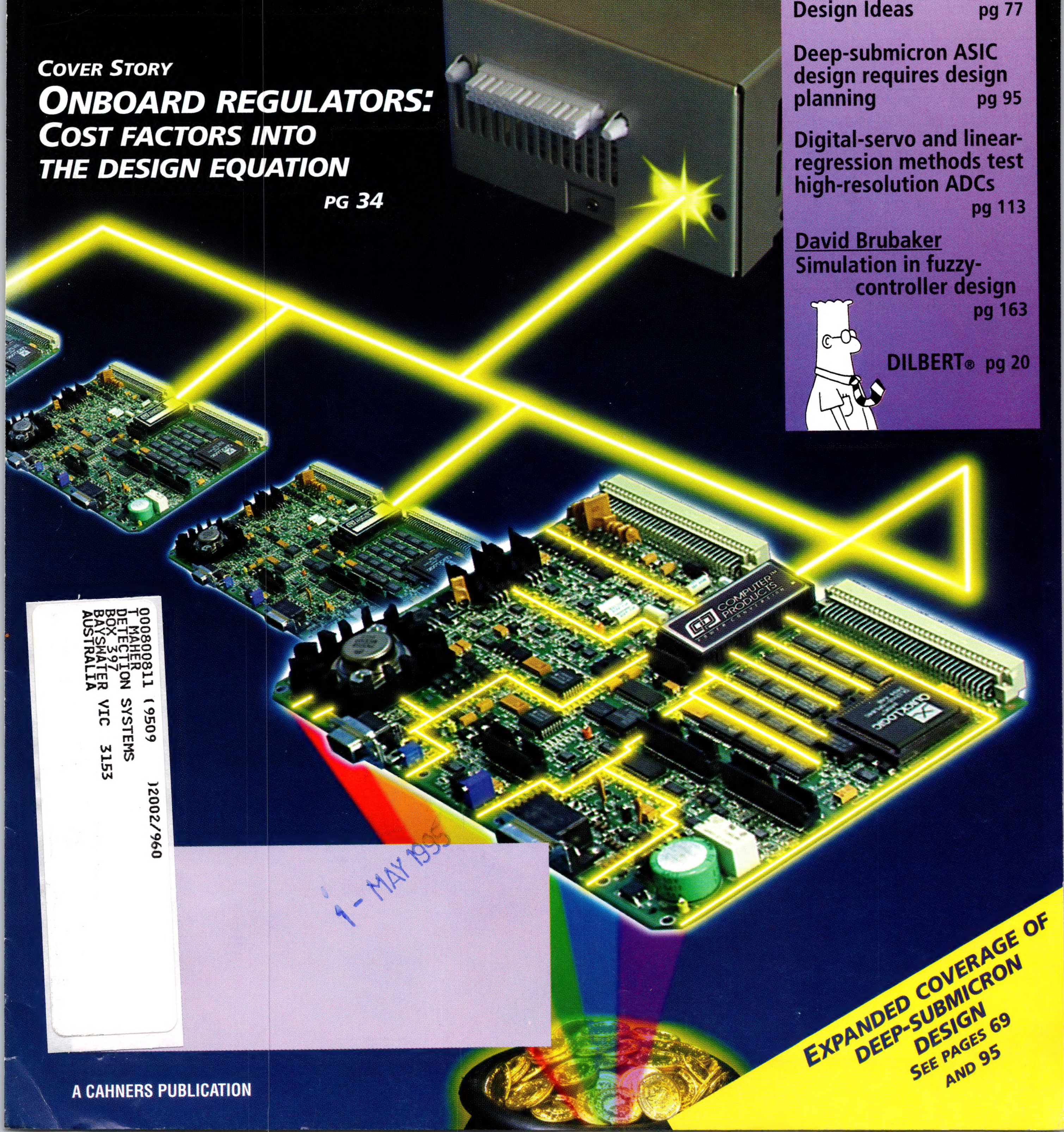
THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

FEBRUARY 16, 1995

COVER STORY

ONBOARD REGULATORS: COST FACTORS INTO THE DESIGN EQUATION

PG 34



EXPANDED COVERAGE OF DEEP-SUBMICRON DESIGN

SEE PAGES 69 AND 95

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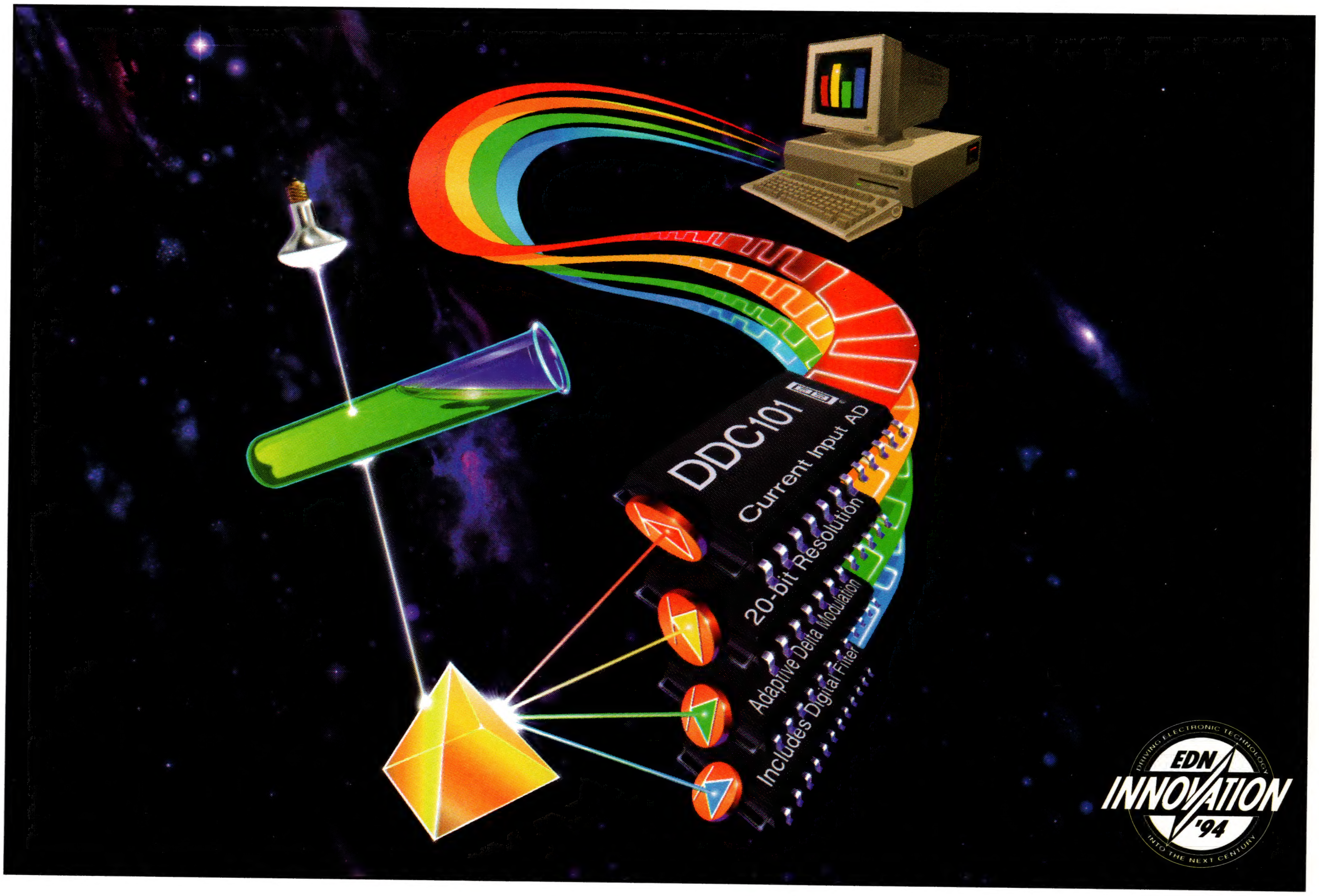

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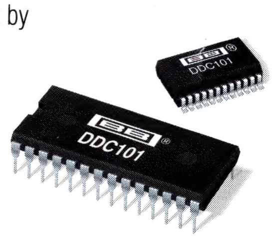

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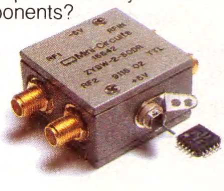

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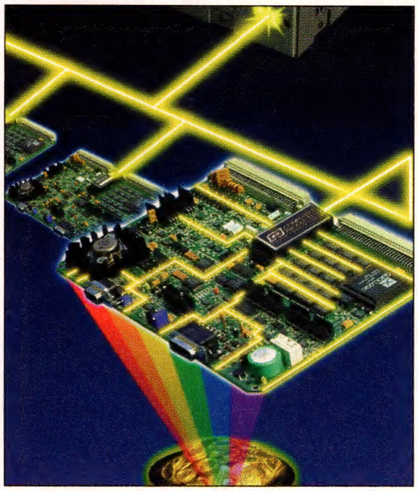

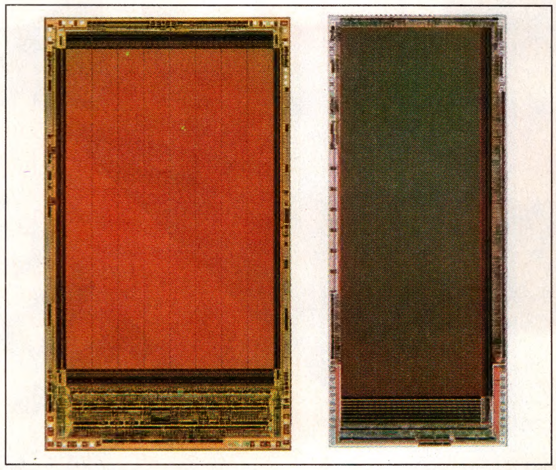

EDN

DESIGN FEATURES

Out in Front

EDN Design Ideas

EDN Columnist

EDN Products

EDN Departments

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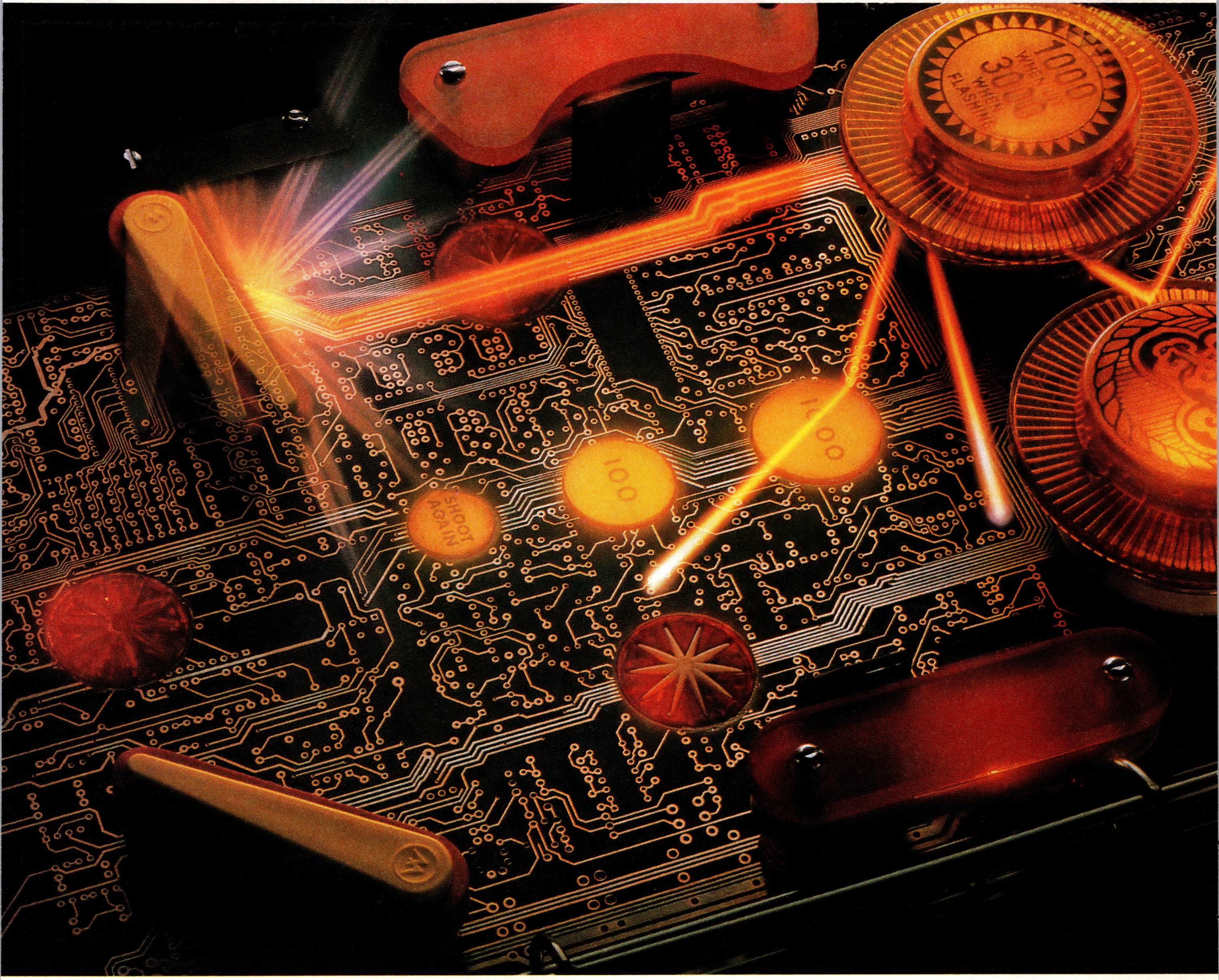
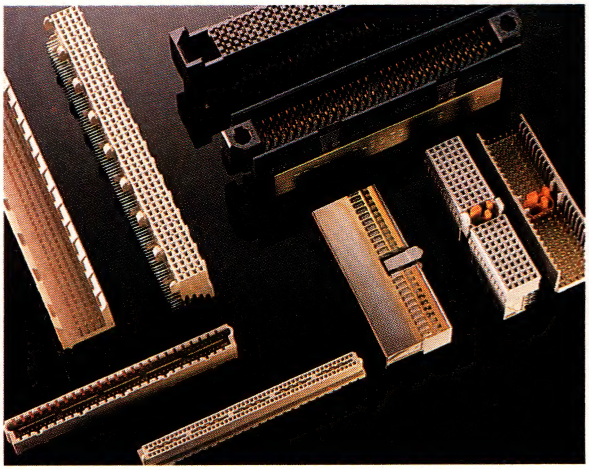
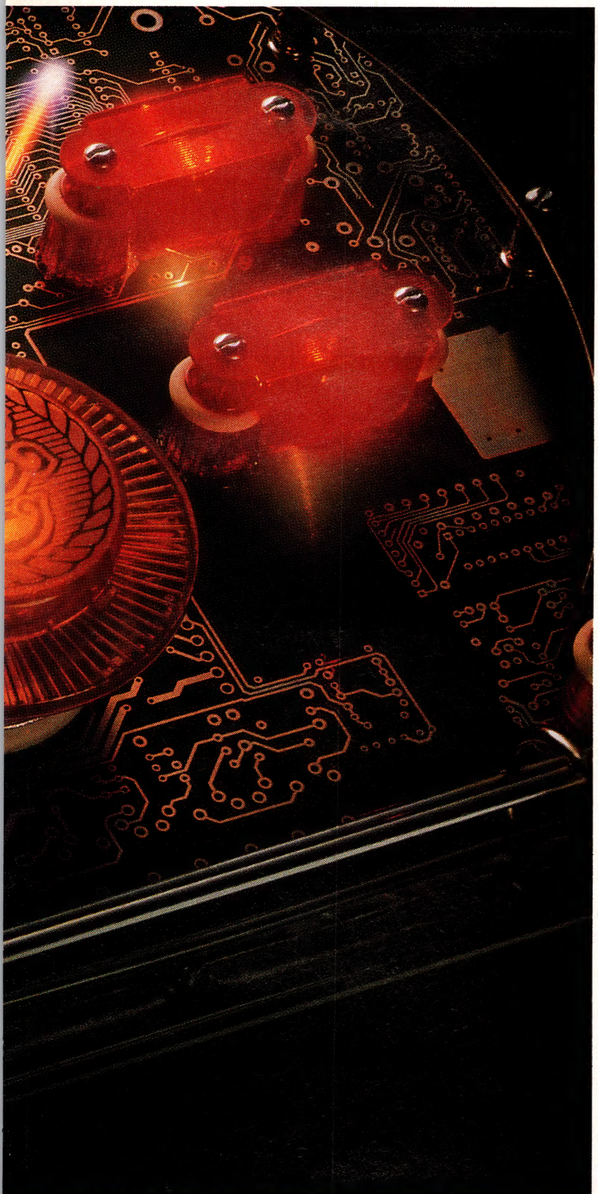
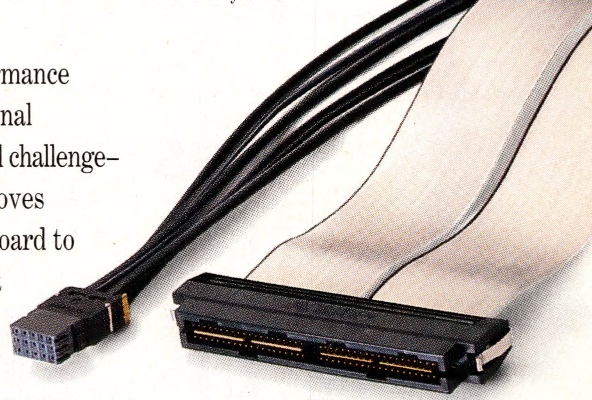
At fast edge rates, the wrong interface takes on unexpected qualities.





AMP high-speed connectors – in hard metric, shielded hard metric, Futurebus, stripline, and microstrip versions – offer a broad range of signal management solutions.





AMP high-speed board-to-cable connectors and cable assemblies minimize reflection, crosstalk, and propagation delay at critical interfaces.

As the demand for performance pushes clock rates up, signal integrity can become a real challenge–especially when traffic moves from board to board, or board to cable. Interconnects that worked last time around suddenly act a lot like bumpers and flippers when your signal hits them. Fortunately, expert interconnect help is available.

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Our high-speed and controlled-impedance interconnect solutions are engineered for hassle-free implementation, even with edge rates pushing 250ps. Our board-to-board selection includes high-density open pin field types (shielded versions available), plus stripline and microstrip styles that allow you to match characteristic board impedances to minimize crosstalk, reflection, and groundbounce. Our board-to-cable selection includes precision miniature coax and transmission line offerings to maintain signal integrity with minimum propagation delay.

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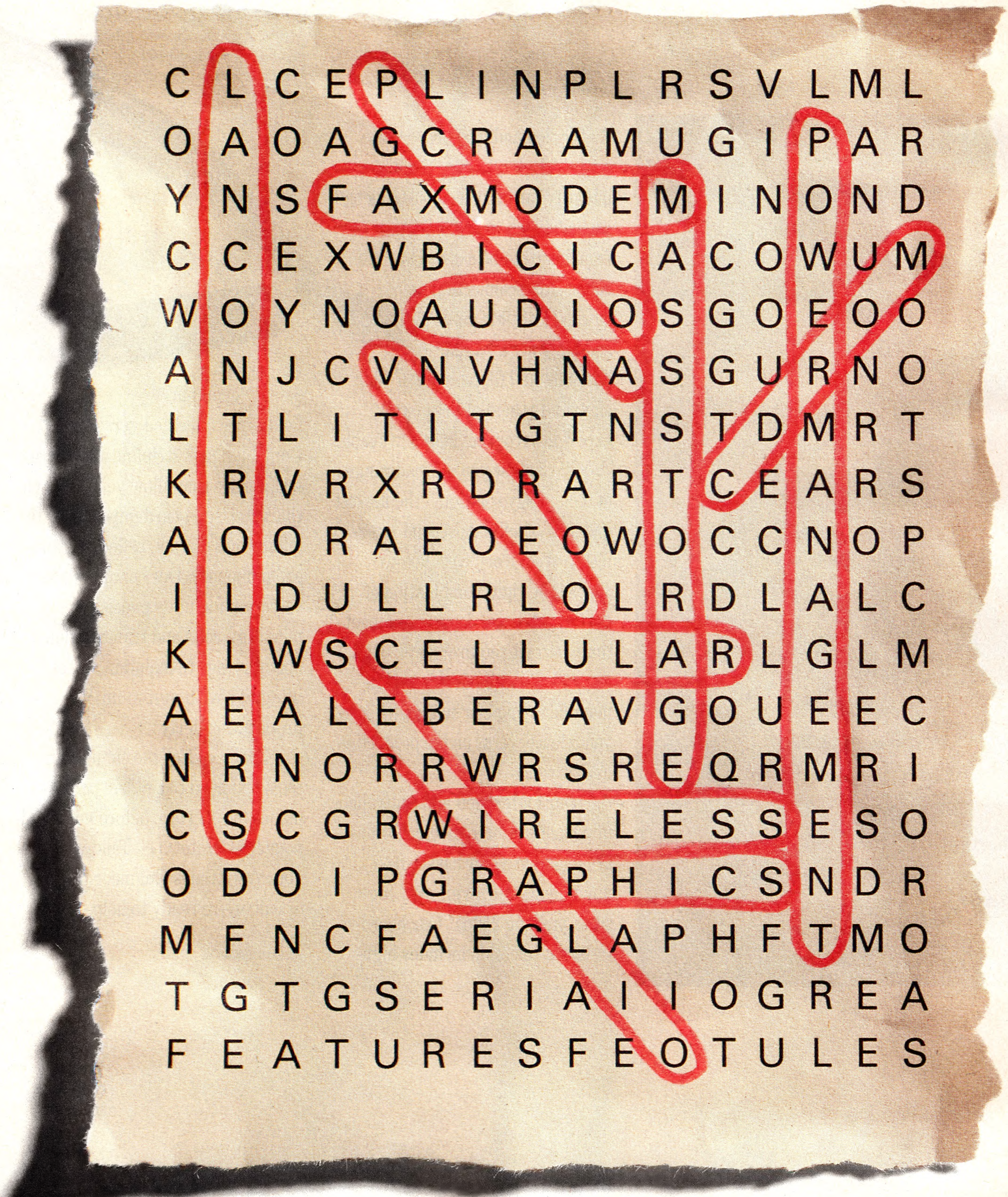
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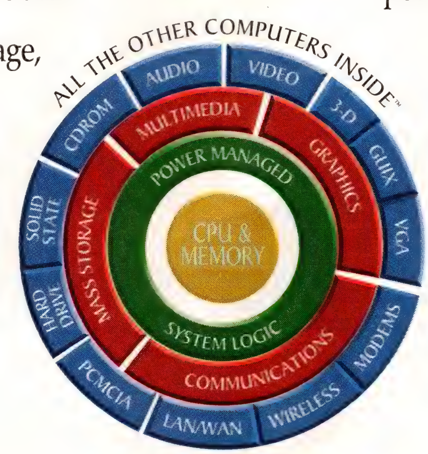

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EDITORIAL | OPINION

Revisiting Decade 90: packaging

In early 1988, I wrote a five-part series called "Decade 90: the future of system design. In it, I tried to forecast the major technological trends that would shape our industry in the 1990s. This is the fourth in a series of five mid-decade editorials looking at how close the predictions came.

The fourth "Decade 90" article addressed new packaging technology for the electronics industry. In this article, you could find every major packaging trend that has now come to dominate the industry. The article opened with a full-page shot of a National Semiconductor IC in a tape-automated bonding (TAB) package. True, few ICs today come in TAB packages, but, with the introduction of Intel's 75-MHz Pentium μP in TAB, you'd have to call the technology mainstream. Incidentally, Epson has been packaging Intel's 80386 and 80486 μPs in TAB packages for years in the Cardio PC-in-a-credit-card products. The high pin counts and low lead impedances of TAB technology suit it well to today's dense, high-speed circuits.

Similarly, "Decade 90" discussed multichip modules (MCMs), which have become far more common today than they were in 1988. A silicon-on-silicon MCM technology developed by Mosaic Systems looked very advanced in 1988, but Ross Technology's HyperSPARC multidie package uses a silicon-substrate, silicon-on-silicon MCM technology. This technique allowed the company to pack a 110-MHz, 6-million-transistor CMOS processor with 256 kbytes of second-level cache memory into one 131-pin PGA package. It's still not cheap, but this processor is for high-end workstations, not high-end military or space hardware.

My favorite packaging technology of the future was the coffee-can computer developed at the Rome Air Development Center (at Griffiss Air Force Base, New York). This technology took whole wafers, deposited solder-covered gold microbridges across their tops and bottoms, and then created a system by stacking, compressing, and heating several wafers. The contacting microbridges made the connections between wafers. No, we don't see that exotic 3-D, wafer-scale chip-packaging technology in use today, but we certainly do see 3-D chip-packaging technology routinely in use at companies such as Densepac Microsystems and Electronic Designs Inc. These companies use the technique to boost the densities of memory ICs beyond what today's monolithic fabrication technology can produce.

Clearly, the advances I forecast in the "Decade 90" packaging article all came to pass before we made it halfway through the decade. IC speeds, power-dissipation requirements, and pin densities continue to press packaging designers, who continue to develop innovations, such as copper heat spreaders and ball-grid arrays. Surface-mount-package lead pitches continue to shrink (coincidentally all but wiping out the electronic hobby industry, but that's another editorial). Somehow, we've stuck by the indomitable edge connector—even with today's "hot" PCI bus—but there are a few alternatives, such as board-stacking connectors and two-piece connectors.

The future of electronic packaging from here to the end of the decade isn't nearly as clear. Today's IC packages seem able to handle incredible densities, such as Ross Technology's HyperSPARC processor, and high speeds, such as the 500-MHz Rambus technology. It may be that we have all the packaging technology we need for the next five years, but I wouldn't count on that.

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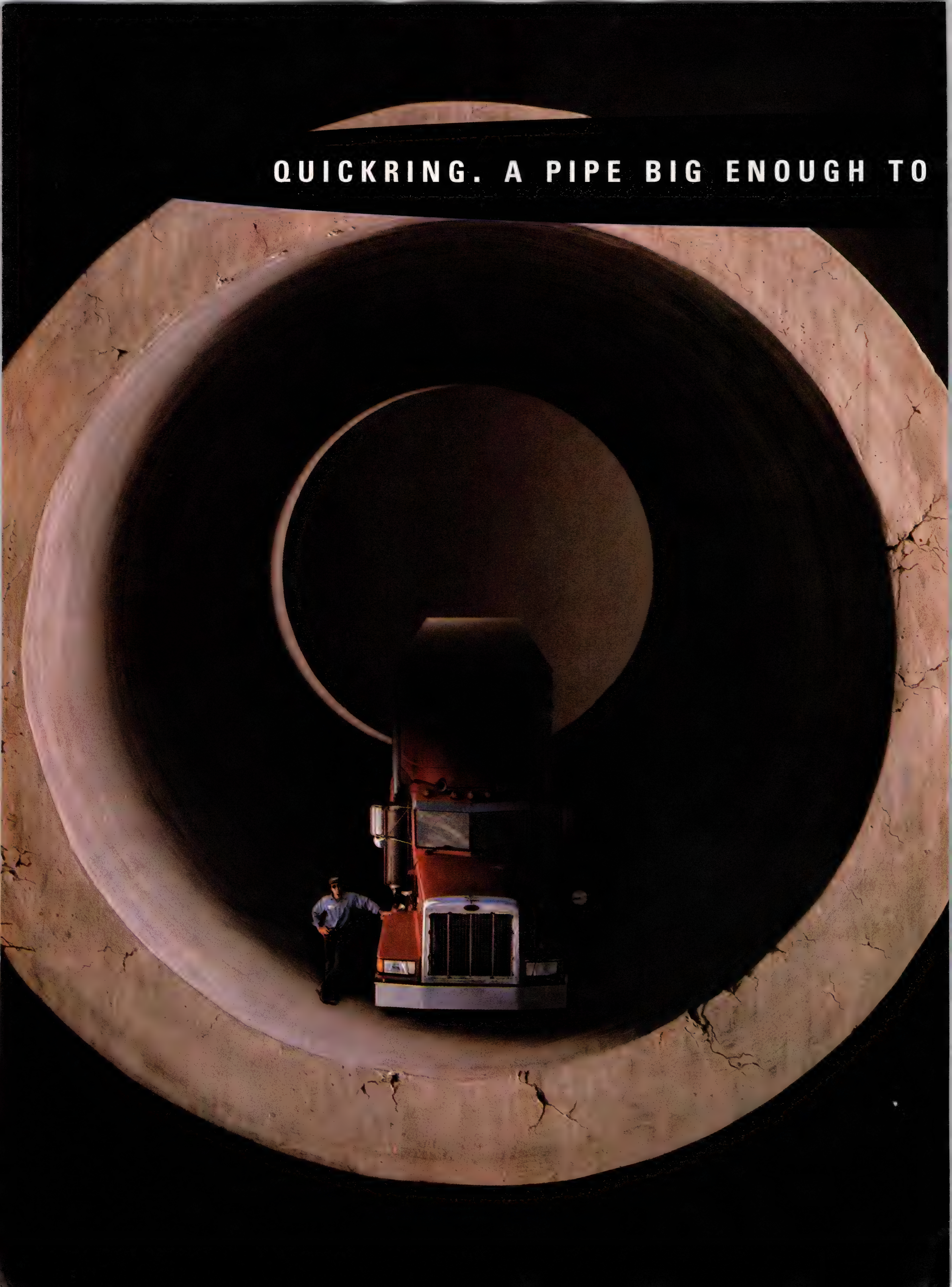
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CIRCLE NO. 105

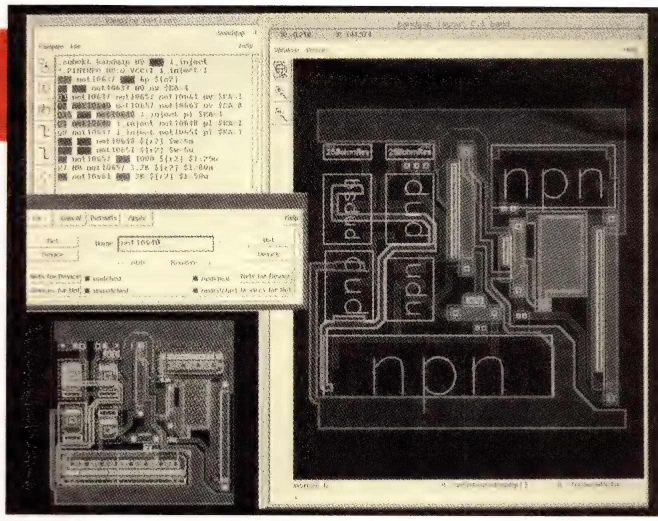
MAJOR EDA PLAYERS AND A START-UP ROLL OUT NEW WARES

FEB 6 MUST HAVE BEEN A DAY OF HARMONIC convergence for the electronic-design-automation (EDA) industry. On that day, two of the major players and a start-up all decided to roll out their latest offerings. Cadence Design Systems introduced Vampire, the industry's first hierarchy-neutral verification system for deep-submicron IC designs. Synopsys jumped into a new arena by introducing DesignSource and HDL Advisor, two products that support a design style that the company calls "Source-Level Design." Meanwhile, start-up vendor Escalade rolled out DesignBook, a high-level ASIC-design package. One of DesignBook's key features is the ability to expertly drive logic-synthesis tools to create logic tailored to your design constraints.

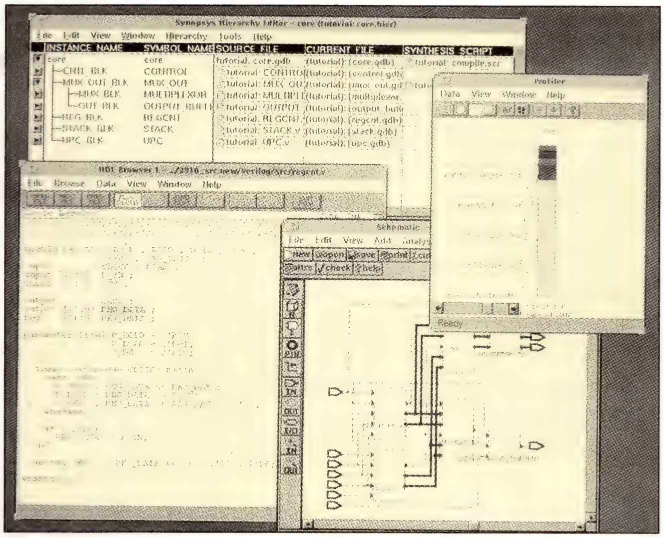
Cadence isn't new to the design-verification market. Its Dracula and Diva packages for digital and mixed-signal ICs are well-known. However, these products are for flat designs or flat pieces of hierarchical designs. With the advent of deep-submicron, multimillion-transistor ICs, flat-design verification is reaching its limits. Vampire employs what the company dubs "auto-adaptive" verification, which analyzes and selectively flattens a hierarchical design to provide accurate verification of large designs in a short time. The company claims that the product verifies designs two to 100 times faster than does flat verification, depending on the task. The product comes as a $75,000 layout-vs-schematic module and as an $85,000 design-rule checker.

Synopsys, the well-known logic-synthesis vendor, is new to high-level design. With its Source-Level Design family of products, the company is trying to do for HDL-based IC development what compilers have done for software development—namely, keeping designers at a high level of abstraction for a long time. DesignSource, the first component of the package, incorporates two graphical editors for Verilog and VHDL and a graphical structural editor for entering high-level (above the HDL descriptions) block diagrams. These graphical editors provide graphical control of operations, such as design linking and swapping alternative architectures. DesignSource also captures associated design information, such as scripts and test benches. HDL Advisor, the companion product, contains an analysis engine, which analyzes the implicit structure of HDL source code; generates structural diagrams showing connectivity, levels of logic,

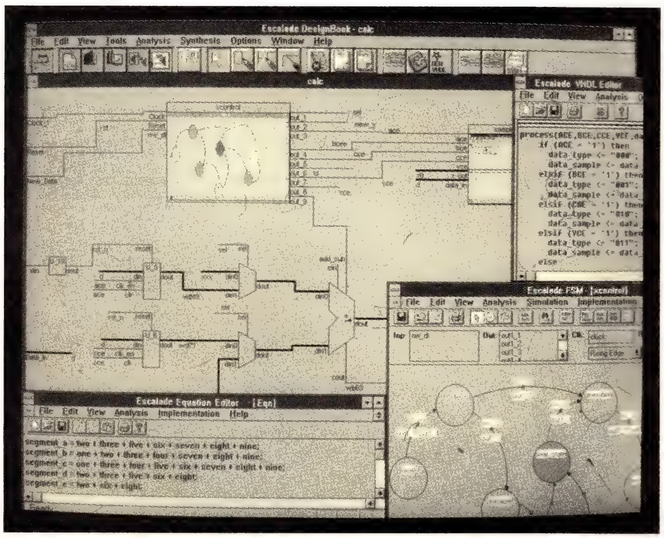
(Continued on pg 20)



Vampire, a hierarchy-neutral design-verification tool from Cadence, handles large ASICs through an adaptive algorithm that selectively flattens designs for maximum speed.



DesignSource and HDL Advisor, part of a new family of Source-Level Design tools, take Synopsys into a new segment of the EDA market.



A suite of graphical editors in DesignBook from Escalade allows you to use multiple design paradigms to enter a design and associated constraints.

generic component counts, and component fan-in and fan-out loads; and correlates postsynthesis timing, area, capacitance, and power data. DesignSource costs $17,000, HDL Advisor costs $24,000, and a package including both products costs $34,000.

Newcomer Escalade is focusing on the high-level design portion of the EDA market with DesignBook, a suite of design tools running under Microsoft Windows or Sun OS. The tool set incorporates several design editors creating what the company calls a "multiparadigm-design environment." These design editors comprise a graphical editor for state-machine design, a block-level design editor for data-path design, an equation editor for Boolean entry, and a VHDL editor. A stimulus-and-timing waveform editor and a test-bench database allow you to enter constraint information as part of a design. Once you create the design, DesignBook generates HDL code for synthesis. In addition, the product drives the synthesis tool "like an expert," setting the synthesizer's hundreds of command-line switches to optimize the synthesized logic according to your design constraints. Timing feedback from simulation or synthesis tools also appears through the waveform editor. DesignBook also provides interfaces for synthesis software from Exemplar Logic and the V/System VHDL simulator from Model Technology. Interfaces for Verilog simulators and Synopsys logic-synthesis tools should be available in June. The company plans to provide other tool interfaces based on customer demand. Prices for the Windows and Sun OS versions start at $14,500 and $25,000, respectively.—Steven H Leibson

Cadence Design Systems Inc, San Jose, CA, (408) 943-1234. **Circle No. 461**

Escalade, Sunnyvale, CA, (408) 481-1300. **Circle No. 462**

Synopsys Inc, Mountain View, CA, (415) 962-5000. **Circle No. 463**

Low-cost microcontrollers provide flash reprogramming

Atmel has expanded its flash-based microcontroller lineup with cost-reduced versions of the 8051. In 20-pin PDIP/SOIC packages, the AT89C1051 and AT89C2051 devices contain 1 and 2 kbytes of flash memory, respectively. The integrated flash memory offers a range of benefits—from just-in-time manufacturing to the ability to update the parts in the field. Designers building low-volume systems (fewer than 20,000 parts/year) will find the flash-based microcontrollers more cost- effective than masked-ROM versions, according to Atmel.

The AT89C2051 also offers fully static operation up to 24 MHz at 2.7 to 6V, 128 bytes of RAM, 15 programmable I/O lines, two 16-bit counter/timers, and a UART channel. The AT89C1051 is similar to the other model but offers only 64 bytes of RAM, one 16-bit counter/timer, and no UART. Price of the AT89C2051 in a PDIP starts at $3.60 (1000).

—by Markus Levy

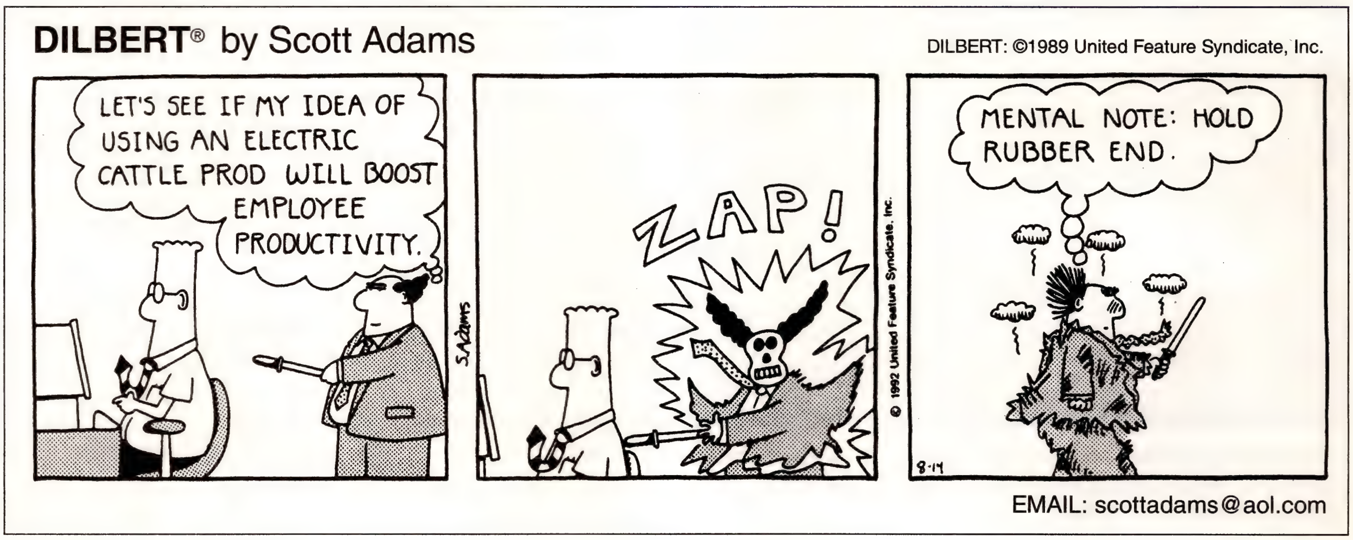
Atmel Corp**, San Jose, CA, (408) 441-0311. **Circle No. 464

Distributors to move Tek test-equipment products

Tektronix Inc, taking a cue from its smaller Pacific Northwest-based rival, Fluke Corp, is embracing distributors as its main channel for selling test-and-measurement products priced below $5000. This strategy contrasts with Tek's former approach of selling such products directly through its now-abandoned "Tek Direct" catalog. Meanwhile, larger rival Hewlett-Packard Co, through its Loveland, CO-based Personal Measurements Operation, continues with catalog-based direct sales.

Currently, Tek's distributor offerings comprise two product lines—TekTools and TekBench. TekTools are largely handheld and battery-powered. TekBench units, though portable, are ac-powered and intended mainly for bench-

(Continued on pg 22)



top use. TekBench includes the company's TDS 300 digital storage oscilloscopes (DSOs). The TDS 400 family is available from distributors, as well as through the company's direct sales force. Other items available through both channels include accessories, such as scope probes and scope carts.

Tek derives more revenues from the sale of oscilloscopes than does any other company, and scopes constitute the core of the company's distributor offerings. But Tek's distributor products include many types of instruments besides scopes: meters, signal sources, counters, and bench power supplies are a few. Key among the new distributor products are the 20-MHz, two-channel TAS 220 analog scope, which costs $795, the TDS 400A family of 200-MHz, four-channel DSOs (with built-in floppy-disk drives), and the PS252X family of triple-output programmable power supplies (from $1195). Call the following number to locate the distributor nearest you.

—by Dan Strassberg

Tektronix Inc, Beaverton, OR, (800) 835-7732.

Circle No. 465

Intel debuts first member of MCS 251 family

Intel's MCS 251 family, a redesign of the 8051 core, yields significantly higher performance than the 8051 and maintains pin and binary-code compatibility with the older device. The register-based architecture includes a 16-bit internal code bus and 40 accessible register bytes as a mixture of 8-, 16-, or 32-bit registers. Intel has also added register-to-register instructions, and you can use all available registers as data pointers, unlike the 8051, which provides only one data pointer. The MCS 251 also contains a three-stage pipeline: instruction fetch or decode, address generation or data fetch, and execution or write-back. Although the original 8051 core runs at 12 clocks per machine cycle, the 251 needs only two clocks. The device also offers 24-bit addressing that yields access to a 16-Mbyte memory space. The device's 64-kbyte extended stack space and additional stack instructions provide better C support than does the 8051.

The first family member, the 8xC251SB, offers 1 kbyte of data RAM, 16 kbytes of ROM or one-time-programmable ROM, a programmable counter array for real-time compare/capture, high-speed I/O and PWM capabilities, a watchdog timer, and 0- to 16-MHz operation at 5V. ROMless versions are also available. The ROM version comes in a 44-pin PLCC and costs $7 (100,000).—by Markus Levy

Intel Literature Center, Mount Prospect, IL, (800) 468-8118. Circle No. 466

EPLD SPECIFIES 7.5-NSEC PROPAGATION DELAY

The XC73144, the latest member of Xilinx's XC7300 logic family, boasts 3500 gates and a propagation delay of 7.5 nsec.

The XC73144 erasable PLD (EPLD) from Xilinx specifies a pin-to-pin propagation delay as low as 7.5 nsec and boasts more than 3500 usable gates. The device can easily integrate the equivalent of 16 22V10 PALs. Output drive is 24 mA, and the unit's I/O interface accommodates 3.3 or 5V logic. The device complies with the Peripheral Component Interconnect (PCI) standard, acting as a flexible PCI bus interface to accommodate the functions for an initiator or a target interface.

The XC73144 also includes a universal-interconnect matrix, which provides access to all on-chip logic resources and guarantees routability. Once you create a design, you can lock the resultant pinout through successive iterations, as long as the logic still fits into the macrocell.

The device comes in a 160-pin PQFP or a 225-ball-grid-array package. The company's XEPLD EPLD-translator-development software supports the device, which comes in 7.5-, 10-, 12-, and 15-nsec speeds. Price for a 160-pin PQFP version is $59.90 (100).—by John Gallant

Xilinx, San Jose, CA, (408) 559-7778.

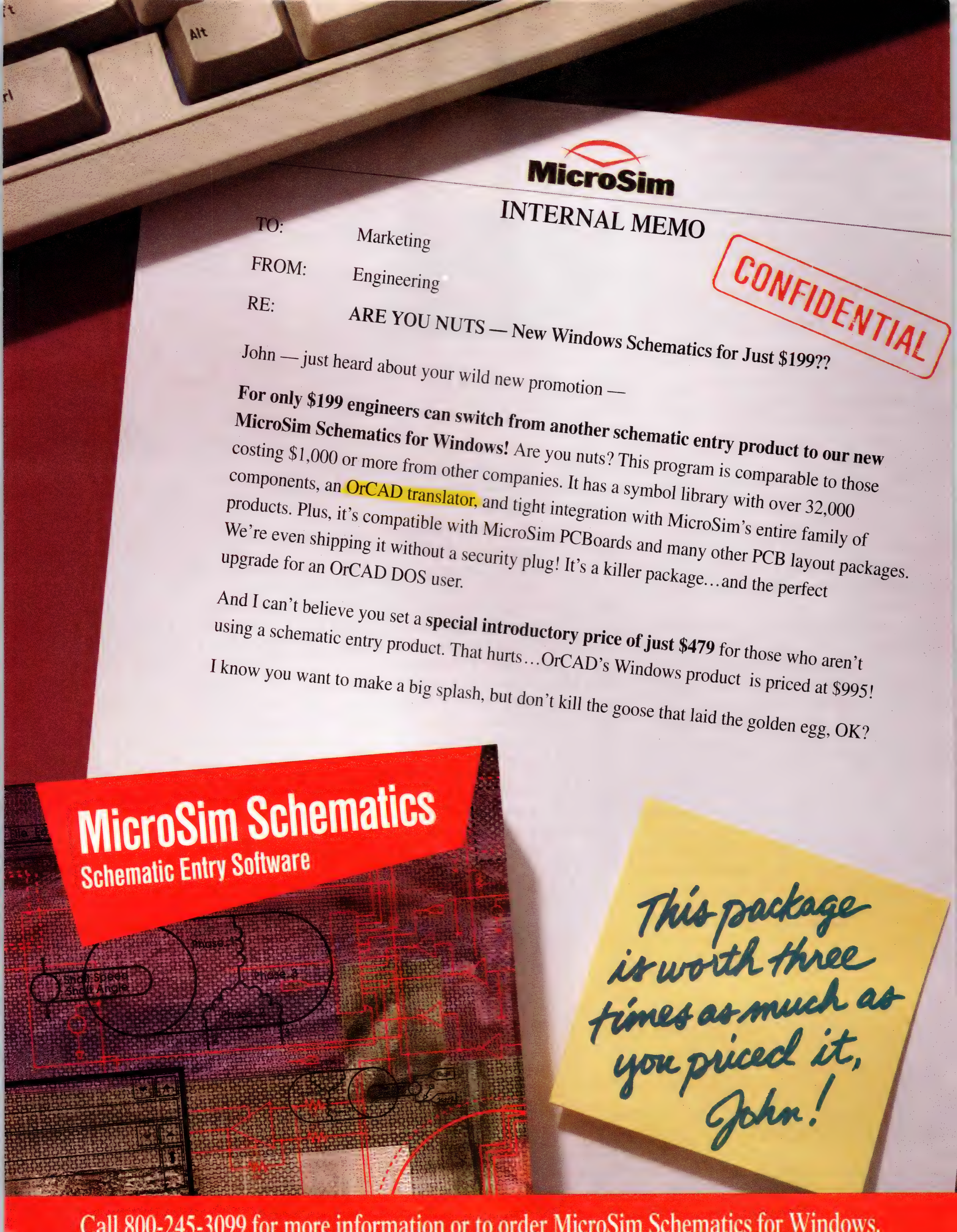
Circle No. 467

PRODUCT REVIEW

Mouse replacement is just right for lefties

Despite major flaws, Cirque's $99 (list price) Glidepoint pointing device can replace a mouse. The unit has several attractive features, the most notable of which is that its only moving parts are its pushbuttons. The Glidepoint's $2\frac{3}{8}\times3\frac{5}{8}\times\frac{7}{16}$-in. dimensions make it much smaller than a mouse. In addition, you don't move it around as you do a mouse, so it takes up considerably less desk space. On the unit's upper surface is a 1.5×2.25-in. touch-sensitive pad. Moving your finger around the pad has the same effect as moving a mouse. Because the pad uses capacitive position sensing, a very light touch suffices. Adjacent to the touch pad, on the edge of the unit that normally faces

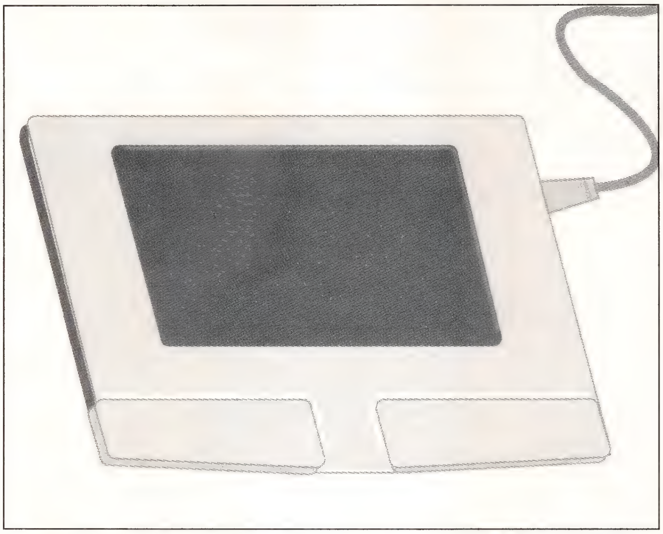
(Continued on pg 24)



CIRCLE NO. 204

you (most users would refer to this edge as the "bottom"), are two pushbuttons whose functions replicate those of a two-button mouse's left and right buttons. You can also simulate clicking a mouse's left button by lightly tapping the touch pad with your fingertip.

You have to get used to the Glidepoint, but, once you do, it becomes a satisfactory replacement for a mouse without a mouse's most obvious shortcomings—an insatiable appetite for desk space and a propensity for having its cord tangle up in objects on the desk. So far, I haven't been tempted to return to using a conventional mouse. However, I am left-handed, and using the Glidepoint is easier for lefties than for righties.



In addition to being smaller than a mouse, Cirque's Glidepoint pointing device does not require you to move it around, so it takes up little desk space.

Even though I find the Glidepoint useful, I am appalled that anyone would even think of marketing a pointing device that is so dreadful ergonomically. You use your index finger to point, and you will want to operate the buttons, which lie at the "bottom," with your thumb. Unfortunately, most people have only one thumb on each hand. So, if you're right-handed, pushing the right button requires moving your hand off the Glidepoint or tucking your thumb under your hand. Either technique is inconvenient enough to discourage a lot of people. Lefties experience similar problems in reaching the left button. For them, switching the functions of the left and right buttons is essential. The Windows Control Panel makes switching easy.

Cirque wouldn't have to increase the Glidepoint's costs at all to make its use much more convenient. All the company would have to do is place one button (the "left" one) on the edge that contains the current unit's two buttons and move the other button to the opposite edge (the "top"). With this layout, using either hand, you could point with your index finger while pushing the "left" button with your thumb or the "right" button with your middle finger.

By taking advantage of Windows' ability to interchange the functions of the left and right buttons, lefties can either click or hold down the "left" button (actually, the button on the right) with their thumb and simulate a right-click by tapping the touch pad. The inability to easily hold down the "right" button isn't a problem; few Windows software packages use right-click-and-drag operations. Unfortunately, the option of right-clicking by tapping the pad is not available to righties; at least with Windows' standard mouse driver, tapping produces the same effect as clicking the left button. Since righties won't want to interchange the button functions, right-clicking isn't as convenient for them as it is for lefties.

The Glidepoint Combo Version, which comes with a nine-to-six pin cable adapter, can plug into either a serial port or a PS/2 mouse port. It works with standard Windows and DOS mouse drivers. It also works with a Logitech DOS driver. The DOS/Windows driver that comes with the Glidepoint is another story, however. When I installed it, the driver interfered with software I use to enhance the Windows File Manager and caused Windows to behave strangely. Deinstalling the Glidepoint drive would have been difficult, if not impossible, had I not been able to edit several .BAT and .INI files using a DOS word processor that I could invoke from outside Windows. Moreover, Cirque's documentation provides incorrect information on where to find one of these files.

—by Dan Strassberg

Cirque Corp, Salt Lake City, UT, (800) 454-3375. **Circle No. 468**

ADLE licenses Commercial-Free. Arthur D Little Enterprises (ADLE) has awarded VCR manufacturer Thomson Consumer Electronics the first license to produce VCRs featuring ADLE's Commercial-Free technology. ADLE introduced the technology last year ("Skip the commercials," *EDN*, Feb 3, 1994, pg 14). Commercial-Free identifies and "marks" commercials; when a user plays back a marked tape, the VCR automatically skips the commercials. **Arthur D Little Enterprises Inc**, Cambridge, MA, (617) 498-5000.

Microchip's serial EEPROMs qualify at 10 million cycles

At 10 million cycles, Microchip's EEPROMs are taking on RAM capabilities. Customer demand for higher quality and endurance has driven this level of performance, which the company has striven for many years to guarantee. An independent test facility, Integrated Circuit Engineering Corp (Scottsdale, AZ, (602) 998-9780) verified the 10-million-cycle qualification (at room temperature).

Although, many applications will never need to cycle the

(Continued on pg 26)

EEPROM devices to 10 million cycles, system designers still appreciate the assurance that their products will not fail in the field. On the other hand, many applications will take advantage of the high endurance these devices offer. It will be interesting to witness what doors the extended-endurance devices will open. Microchip offers this level of endurance throughout the entire serial-EEPROM product line at no additional cost. The company also offers a $149 serial EEPROM designer's kit that lets you check out the devices for yourself.

—by Markus Levy

Microchip Technology Inc, Chandler, AZ, (602) 786-7200 **Circle No. 469**

FOUR COMPANIES TO OFFER BURST EDO DRAMs WITH 66-PAGE-MODE RATE

Burst extended-data-out (EDO) DRAMs from Hyundai, Micron, Mitsubishi, and Siemens use standard EDO technology and add on-chip burst counters and starting address latches. The devices offer column-cycle times 30% faster than those of standard EDO DRAMs. The DRAMs support both linear and interleaved burst counts and use the #CAS pin to increment the counter. These burst devices come in the same package and pinout types as do fast-page-mode and standard EDO DRAMs; therefore, implementation requires only simple modifications at the chip-set and system levels. Furthermore, the manufacturers will implement the devices as a bond option on standard DRAMs, allowing the new units to take advantage of the same high-volume manufacturing as the older devices. Eight chip-set suppliers plan to support the devices this year.

—by Markus Levy

Hyundai Electronics America, San Jose, CA, (408) 473-9200. **Circle No. 470**

Micron Semiconductor Inc, Boise, ID, (208) 368-3950. **Circle No. 471**

Mitsubishi Electronics America Inc, Sunnyvale, CA, (408) 730-5900. **Circle No. 472**

Siemens, Cupertino, CA, (408) 777-4500. **Circle No. 473**

Voice controller stores 20 minutes of data in flash RAM

Eurom's VoiceChip, a one-chip voice-recording and -playback device, stores as much as 20 minutes of voice data in 1 Mbyte of external flash memory. The device integrates a voice processor, analog I/O, and peripheral support. An 8-bit controller controls all the device's functional units and communication with external systems. The system executes instructions from internal ROM and includes internal RAM for temporary storage and buffering. You can replace the internal ROM and RAM with external devices.

The device also allows you to vary voice compression for each recorded message, and it can address flash-memory arrays as large as 8 Mbytes. The VoiceChip has two serial interfaces: an I^{2}C bus interface and a standard UART serial interface. The analog portion includes a 10-bit ADC and an 8-bit DAC. A sleep mode reduces power consumption.

In stand-alone configuration, the system-bus pins interface directly to a 16-key keyboard and drive a four-digit LCD. A programmable timer generates the backplane clock for the LCD as well as the internal interrupts that the device services. Price is $15 to $19, depending on volume.—by John Gallant

Eurom Flashware Solutions Inc, Santa Clara, CA, (408) 748-9995. **Circle No. 474**

BOOK REVIEW

The elements of board test

Stephen Scheiber's superbly written book, *Building a Successful Board-Test Strategy*, delivers on the promise of its title. If your job is figuring out how to test boards or similar assemblies, you'll find that Scheiber cogently and succinctly describes the issues you ought to consider. He provides in-depth coverage of such recent topics as boundary scan, the VXIbus, and the economics of test. Scheiber neither tries to tell you how to test particular types of boards nor provides great detail on the operation of test systems or the syntax of test-programming languages. Such emphasis would only cause readers to get lost in the trees rather than helping them to understand the forest.

Readers in design might easily question why they should own a book such as this one. Scheiber answers that question early on in his discussion of concurrent engineering. He correctly points out that concurrent engineering is a new name for a mode of operation that savvy managers have been using for decades. An organization or a project team is most effective if every member can appreciate what issues the other team members find really important. Board-test issues *do* influence the way you design products. Short of walking in an experienced test-engineering manager's shoes for a year or more, nothing is likely to bring you closer than this book does to thinking about test issues the way a test manager would. The 286-pg book (ISBN 0-7506-9432-7) costs $44.95.—by Dan Strassberg

Butterworth-Heinemann, Woburn, MA, (617) 928-2500. **Circle No. 475**

Cost per MFLOPS
Cost per MIPS
$50
$5
$0.5
$0.1
1982
1992
2002

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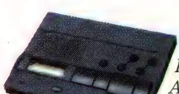
Cellular Phone

	1988	1995
Talk Time	2 hours	3 hours
Size	8"x3"x2"	5.5"x2.3"x1"
Weight	2 pounds	0.5 pound
Price	$1,000	$59-$300



Digital Telephone Answering Device

	1988	1995
Reliability	Tape-Based	Solid-State
Caller ID	No	Yes
Mailboxes	No	Yes
Price	$30+	$40+

Fax Modem

	1988	1995
Baud Rate	2,400 bps	28,800 bps
Capability	Data/Fax	Data/Fax/Voice
Format	PC Half Card	PCMCIA
Price	$300	$350

Hard Disk Drive

	1988	1995
Access Time	60 ms	12 ms
Size	3"x6"x8"	3.3"x2.1"x0.4"
Density	20 Mb	400 Mb
Price	$350	$350

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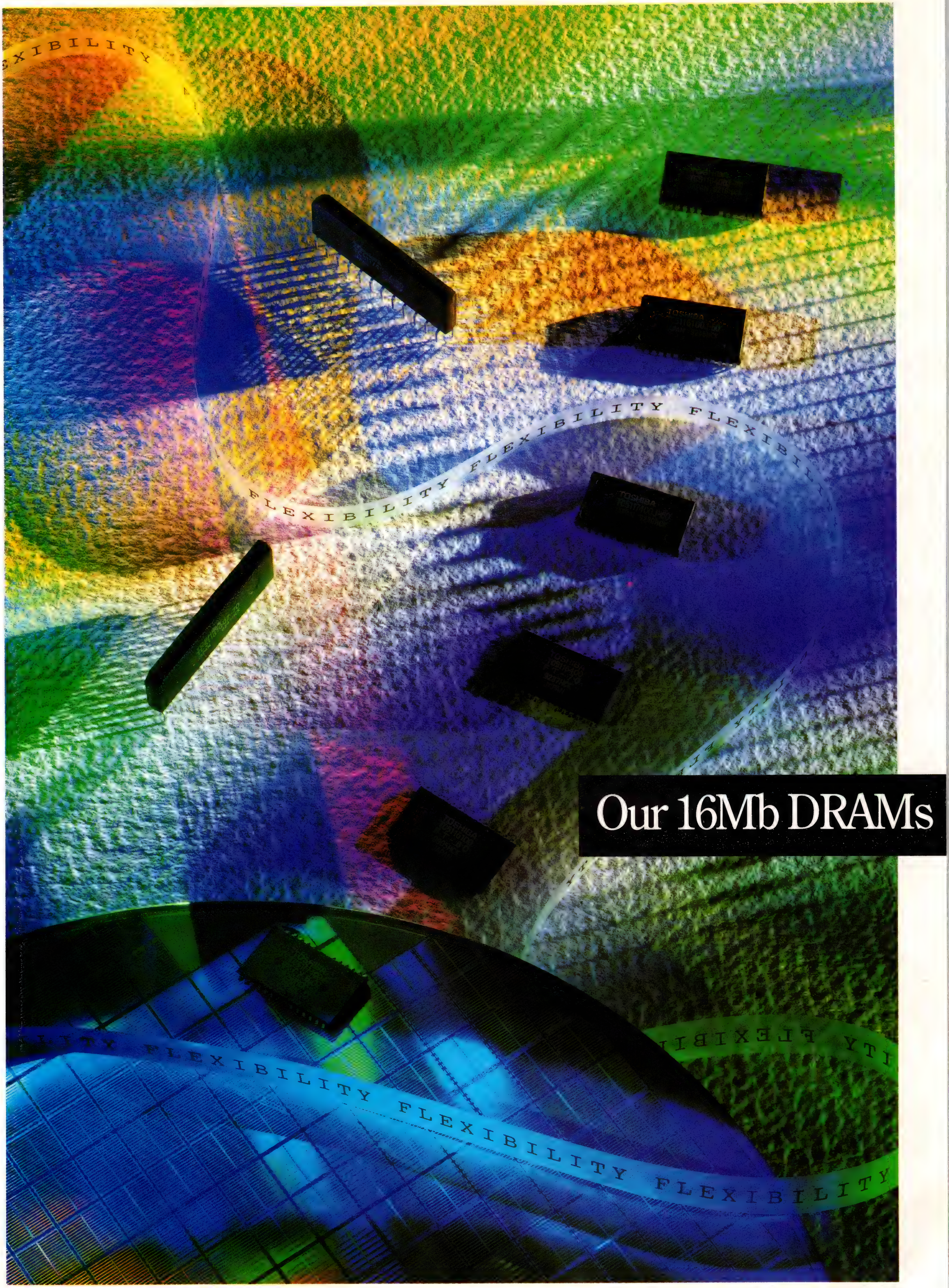
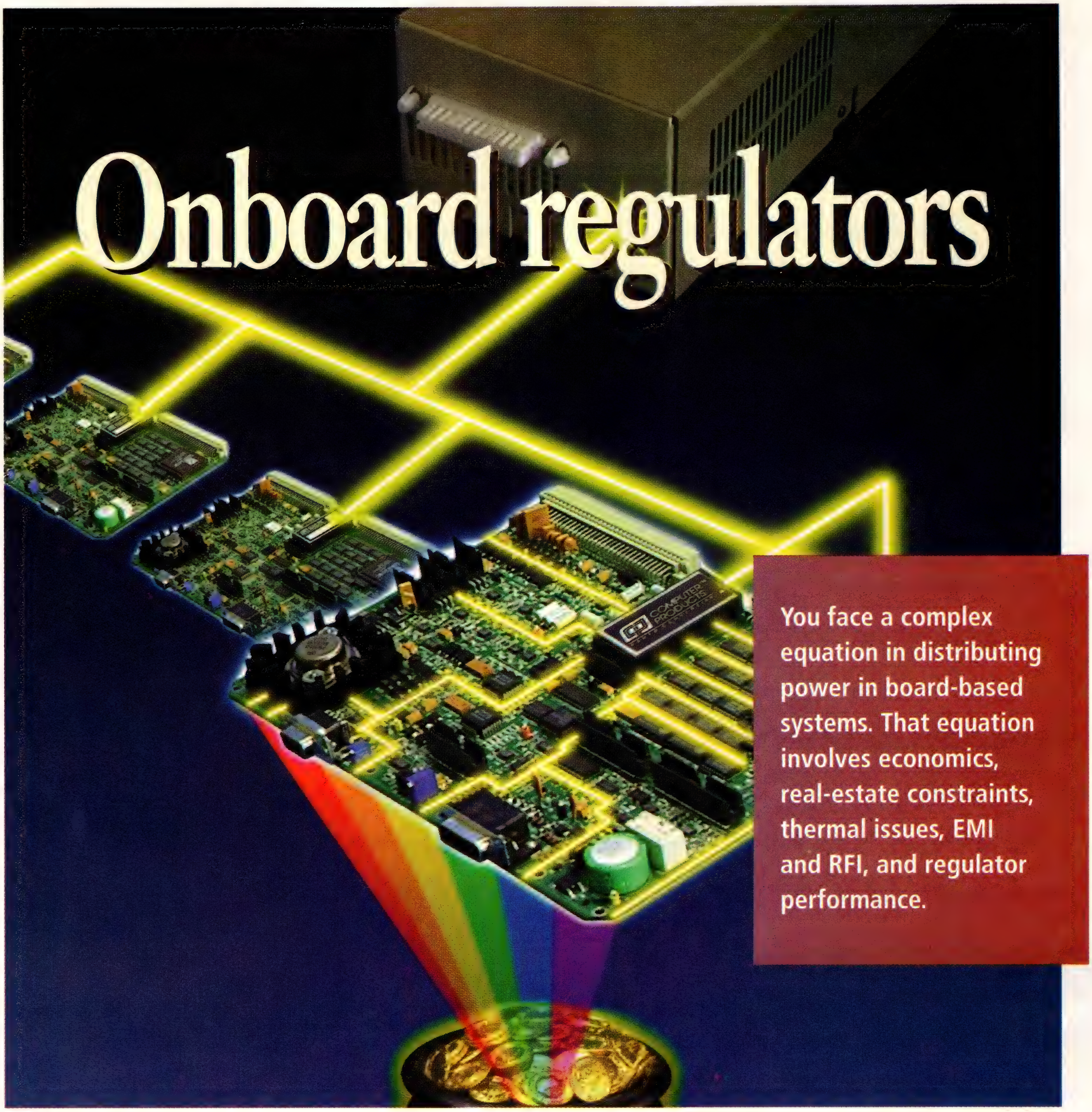

FLEXIBILITY FLEXIBILITY
FLEXIBILITY FLEXIBILITY
Our 16Mb DRAMs

Onboard regulators



You face a complex equation in distributing power in board-based systems. That equation involves economics, real-estate constraints, thermal issues, EMI and RFI, and regulator performance.

BILL TRAVIS, SENIOR TECHNICAL EDITOR

Like "embedded systems," the buzz phrase "distributed power" is likely to evoke sage nods. For, as most designers know, it's the way to go in all but the smallest systems. The concept of providing local, onboard regulators for individual circuits or blocks of circuits is alluring. However, as obvious as the concept of distributed power might seem, the nuts-and-bolts implementation of the concept is not always so obvious. A number of factors enter into the equation (or suite of equations) that governs your choice of regulators:

- Degree of distribution—how "far down" to subdivide the power
- Switching vs linear regulators
- Modular or hybrid vs monolithic regulators
- Conducted and radiated switching noise—EMI, RFI issues
- Real-estate constraints—regulator dimensions, power density
- Thermal issues—heat distribution and removal
- Needed or desirable regulator features—protection, supervisory functions
- External components or modules needed for proper regulator operation
- Cost—total dollars per watt.

The first component in this

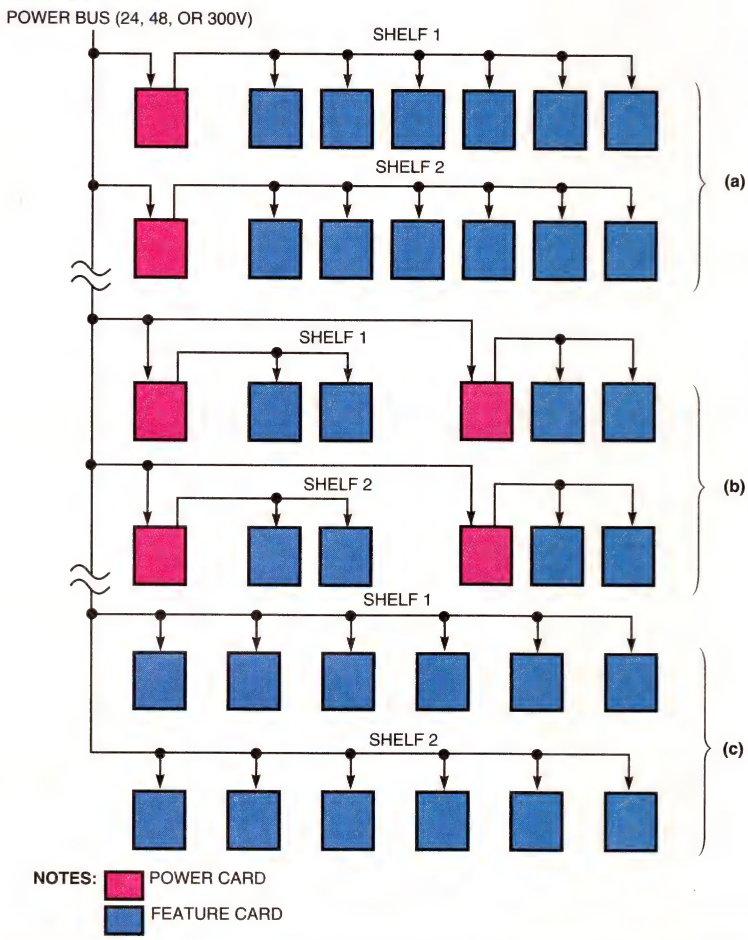
list, the degree of power distribution or subdivision, is a complex issue in and of itself. **Fig 1**, derived from material in **Ref 1**, shows three possible ways to distribute the power in a two-shelf or two-rack system. In **(a)**, a separate card provides power, converted from the 24, 48, or 300V intermediate power bus, for each shelf of feature cards. In **(b)**, four converter cards provide regulated power for small blocks of feature cards. Finally, in **(c)**, each feature card carries its own power converter.

These distribution schemes are alternatives to the time-honored technique of using one centralized ac/dc power supply to supply multiple regulated voltages to the whole system. On the face of it, centralized power is more economical, in terms of dollars per watt, than distributed power. However, because of the custom nature of most systems' voltage and current demands, the design effort for a centralized supply can be long and expensive.

Distributed power has several technical advantages over centralized power. First, the long conductor runs in a centralized-power system can result in high distribution losses and poor point-of-load voltage regulation. Next, power-conversion losses (heat) in a distributed-power system are diffused throughout the system, rather than concentrated in one power-supply chassis or box. Finally, distributed regulators offer you localized monitoring and control of protection, diagnostics, and supervisory functions.

Table 1 gives some relative advantages of each of the configurations in **Fig 1**. Given equal conversion efficiencies for the regulators in all three distribution schemes, the configuration in **Fig 3c** usually yields the lowest losses and the best point-of-load regulation. The lower the operating voltage, the more striking the performance advantages of local regulation. For example, one of the shelves in **Fig 1a** could draw several amperes at 3.3V. This would cause just 0.1Ω series resistance in the power-supply conductor lines or connector system to drop the local supply voltage below acceptable limits.

FIGURE 1



The level of power distribution—shelf-level (a), function-level (b), or card-level (c)—determines your choice of regulators (switching or linear, modular or monolithic) and influences the design of your thermal-management system.

Choose intermediate voltage

Assume you've decided a distributed-power system, whatever the level of distribution, would be optimum for your system. One of the attractive aspects of distributed power is that the central ac/dc power supply can have relatively sloppy accuracy and regulation specs. The intermediate voltage you choose for distribution can have a wide tolerance and fairly gruesome ripple characteristics. In selecting this voltage, you have to make a trade-off involving distribution losses, cost, and safety considerations.

Intermediate bus voltages typically range from 12 to 900V. High voltages have the obvious advantage of low I^2R distribution losses and the use of less copper for conductors because of lower currents. One disadvantage of using high bus voltages is the safety hazard. UL1950 and the European Telecom Standard EN41003 set safety extra-low voltage at 60V, the maximum nonhazardous voltage. Another drawback is that local dc/dc converters with very high input ranges are usually more expensive than those with lower ranges.

Low intermediate bus voltages pose no safety hazards. In some cases (notably, 5-to-3.3V conversion), they allow you to use low-cost, low-dropout linear regulators. The disadvantage is the necessarily higher supply currents, creating the need for more conductor copper. Even with beefed-up conduc-

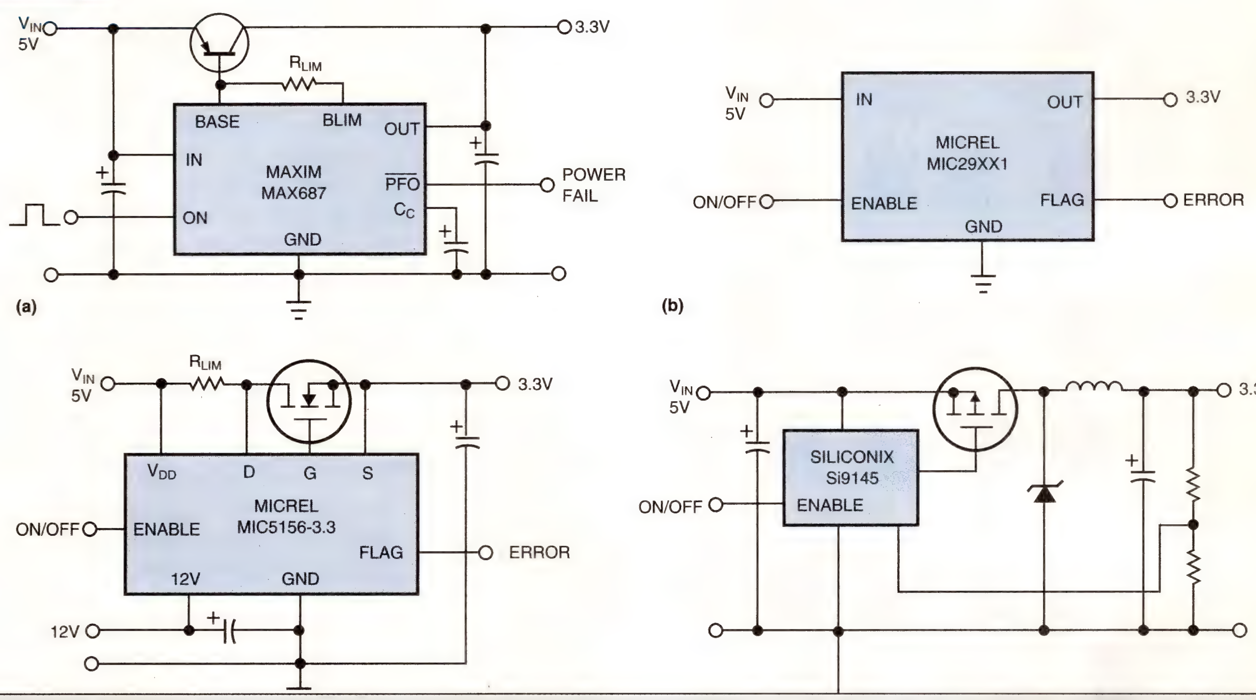
tors, though, the trace, switch, and connector series impedances can produce high distribution losses. Common intermediate voltages are 24V for industrial controls, 28V for military/aerospace, and 48V for telecommunications, and large computer systems.

Returning to **Fig 1**, assume you've selected 48V as the intermediate bus voltage. The task of the power cards in **(a)** and **(b)** and the local converters in **(c)** is to convert this 48V to the required board-level voltages—usually, 5, 12, or 15V or any combination of these, unipolar or bipolar. You'd use a switching regulator to convert down from the 48V intermediate-bus voltage; linear regulation would entail a horrendous

TABLE 1—ATTRIBUTES OF DISTRIBUTION SCHEMES

Configuration	Regulation, busing issues	Reliability issues	Diagnostics	Thermal-load distribution
Per shelf (Fig 1a)	Needs robust power bus to avoid copper losses	Power-card failure shuts down entire shelf; however, N+1 or N+x redundancy easy to configure	Failure easily traceable to particular shelf; hot-plug replacement possible	Heat sinking and forced air-flow usually required for high-power, shelf-level dc/dc converters
Per function block (Fig 1b)	Better regulation, lower conductor losses than **1a**	Power-card failure affects only local function; also, N+1 or N+x redundancy easy to configure	Failure easily traceable to function block; hot-plug replacement possible	Decentralization of heat concentration allows convection cooling of some power cards
Per card (Fig 1c)	Best regulation, lowest conductor losses	Redundancy difficult to configure; however, power-card failure shuts down only one feature card	Failure easily traceable to specific feature card	Maximum diffusion of thermal load; allows convection cooling or minimal forced-air cooling

FIGURE 2



Monolithic regulators and controllers offer you several ways of configuring a 3.3V power system. The low-dropout linear regulators in (a) and (c) use external discrete devices; the IC in (b) contains an integrated super-beta pnp transistor to provide the same function as the circuit in (a). The switching regulator in (d) uses an external MOSFET (two, in a synchronous connection) to configure a high-efficiency converter.

waste of power. The switching-vs-linear issue is not so clear-cut, however, in converting from 5 to 3.3V.

Most digital or mixed-signal systems have ample availability of 5V power. If you need 3.3V at a certain location—for instance, for an embedded high-speed µP—you must choose how to convert the 5 to 3.3V and meet the necessary requirements for accuracy, protection features, pc-board real estate, and cost. You must also decide whether the application calls for a modular, a hybrid, or a monolithic converter. **Tables 2** and **3** (see pgs 46 to 49) give some representative modular and monolithic onboard regulators, both switching and linear.

In this 5-to-3.3V example, you must also decide if a complete, one-package regulator or one that requires external components is more appropriate. Almost all the modular or hybrid regulators in **Table 2** are complete, drop-in converters with such features as current limiting and overtemperature shutdown. Depending on the power level you need, the cost starts at around \$1/W. And high modular power densities yield small footprints—2×1×0.45 in. and 1.64×0.36×1.16 in., for example, for a 26.4W (8A) converter.

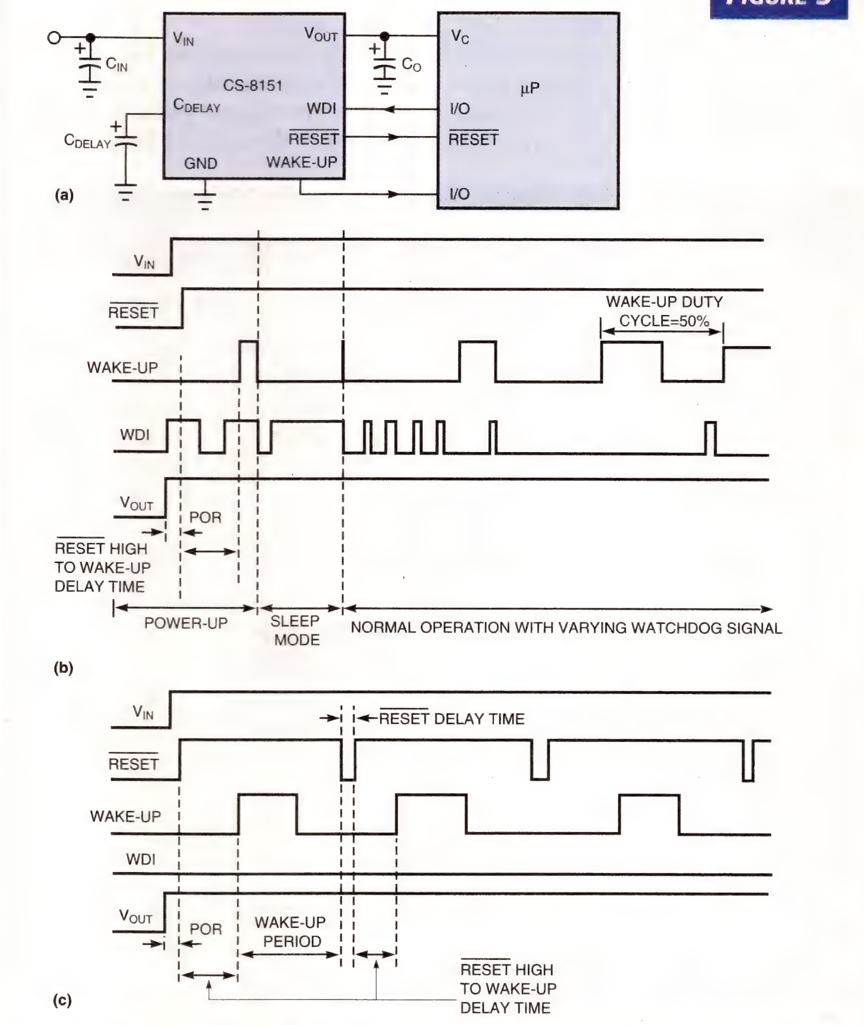
Instead of using a modular or hybrid converter, let's hypothesize you'd prefer to implement the conversion with a monolithic regulator, like one of those in **Table 3**. You might opt to do this to shave some costs or to minimize board space, for example. **Fig 2** shows four possible ways to obtain a regulated 3.3V supply from the 5V bus. The configurations in **(a)**, **(b)**, and **(c)** are linear regulators. In 5- to-3V conversion, "linear" is not necessarily a dirty word. The conversion efficiency approaches 66%. This figure is not a whole lot lower than those for 3.3V switching regulators—at 3.3V, rectifier and switching-element losses become significant and keep conversion efficiency in the low-80 or high-70% region.

The low-dropout (LDO) regulator in **Fig 2a** uses an external pnp pass transistor. The pnp structure is the one of choice in bipolar LDO schemes, because an npn configuration has a dropout voltage of at least 1V ($V_{BE(sat)}+V_{CE(sat)}$). If you have enough input-voltage margin and don't need an LDO regulator, an npn structure is preferable, because all the base-drive current goes to the load and, thus, doesn't subtract from the conversion efficiency. In a pnp circuit, the base-drive current goes to ground. The Maxim MAX687 (**Fig 2a**) supplies at least 10 mA of base drive to the external pnp, so the regulator can supply at least 10×beta mA to the load.

Micrel provides a self-contained version of the circuit in **Fig 2a (Fig 2b)**. The MIC29XXX Series uses an on-chip, super-beta pnp pass transistor to provide LDO voltages. Available in 1.5, 3, 5, and 7.5A versions, the regulators guarantee ±1% accuracy on the 3.3V output. The maximum dropout voltage is 600 mV for all rated output currents. The ground (base-drive) currents are specified at approximately 1% of the load current.

Similar to the circuit in **Fig 2a**, the regulator in **(c)** uses an external pass element. This time, though, the element is an n-channel MOSFET. The dropout voltage is the product of the

FIGURE 3



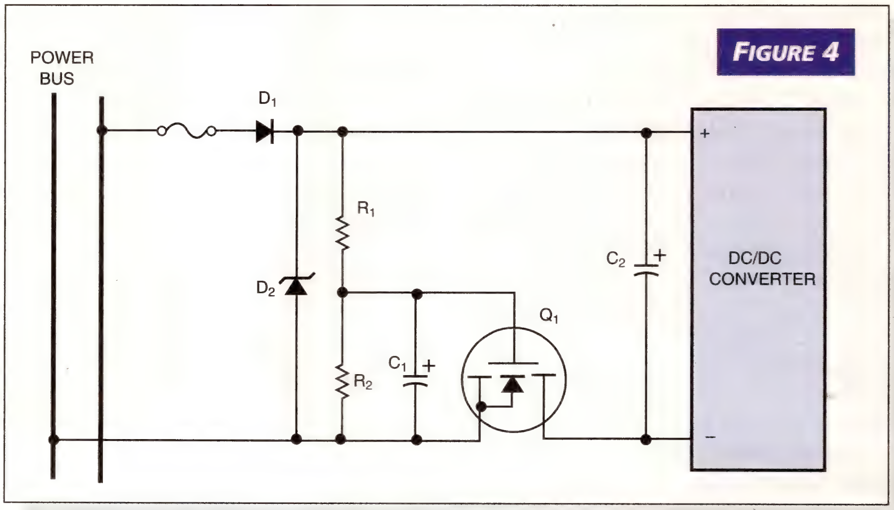
C_{DELAY} in (a) sets the timing for the reset and wake-up functions. In (b), the µP remains in sleep mode after power-up and sends back at least one watchdog signal within each wake-up period. In (c), when the µP fails to send a watchdog signal to the regulator, the CS-8151 issues a reset back to the µP until a wake-up signal appears.

ONBOARD REGULATORS

MOSFET's $r_{DS(on)}$ and the output current, and the output current is limited only by the size of the MOSFET. This configuration uses Micrel's MIC5156, which requires a 12V input to provide gate drive to the MOSFET. Another version, the MIC5157, contains a charge-pump tripler that (with the addition of three external capacitors) provides the gate drive. The advantage of these circuits over the bipolar LDOs is the elimination of the base-drive current. For a load current of 200 mA or lower, Maxim's MAX882 Series integrates a p-channel MOSFET to provide 220-mV dropout voltage at full rated current. Thanks to the absence of bipolar base drive, the quiescent current is only 11 μA.

For conversion efficiency greater than 66%, you need a switching regulator. **Fig 2d** shows how you can configure a step-down buck converter

FIGURE 4



To provide hot-pluggability without worry, this circuit limits large inrush currents, provides reverse-voltage protection, and clamps the regulator's input to a safe level in the event of power-line transients. The fuse limits input power in case of a catastrophic failure within the converter or the power bus.

REGULATORS NEED EFFECTIVE THERMAL MANAGEMENT

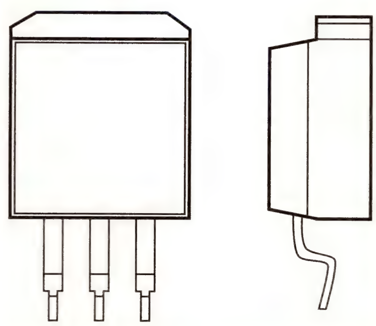
VAD VASCONCELOS AND DAVE HEGARTY, WAKEFIELD ENGINEERING

Just as with other circuit types, onboard regulators deserve careful thermal-management studies in the concept stage of system design. Such studies not only help you achieve the required thermal performance from both the component and the system, but also have an impact on cost, reliability, and manufacturability.

Cost-effective onboard voltage regulation involves a collaboration of electronic designers and their mechanical counterparts, working together to implement new heat-removal products at the board-layout stage. For example, you can replace a regulator in the venerable TO-220 package by one in a surface-mount package, such as the TO-263 from Micrel (**Fig A**) surface-mount package reduces board space and lowers costs through pick-and-place automation. The challenge in cooling such devices is to make the transition from traditional through-hole techniques to surface-mount methods.

A series of surface-mountable heat sinks addresses the cooling requirements of D²Pak, TO-263, and other such surface-mount packages. The heat-transfer mechanism of the 216 Series of heat sinks resembles neither through-hole nor direct-attachment types. The heat sink has no direct contact with the surface-mount device. Instead, heat propagates from the surface-mount device to the pc-board copper pad, which connects to the surface-mounted heat-sink rails. Depending on airflow velocity and direction and heat-sink orientation, this cooling arrangement can more than double the power available from a surface-mount device.

FIGURE A



Easy-to-use, thermally efficient surface-mount packages are displacing the venerable TO-220. Specially designed heat sinks take the heat away from the copper mounting pad.

As an example, assume you must limit the temperature of lead 2 (ground) to 125°C in a 55°C ambient temperature. The temperature difference is 70°C. For 200-linear-ft/minute (lfm) air velocity perpendicular to the heat-sink fins, thermal resistance is 17°C/W. Thus, the allowable device power dissipation is 70÷17, or 4.1W. At 40°C ambient and 400 lfm, the same regulator's dissipation would be more than 6W. Without heat-sinking, the allowable dissipation in this example would be about 2.5W.

To sum up, you must consider the heat-sink selection, interface material, attachment methods, and automation techniques if you want to reduce the total system cost. In some instances, you must weigh the benefits of a custom cooling solution. "Custom" is not the forbidding word it once was; most companies have application engineers who can assist in design, evaluation, and product selection—sometimes at surprisingly low cost.

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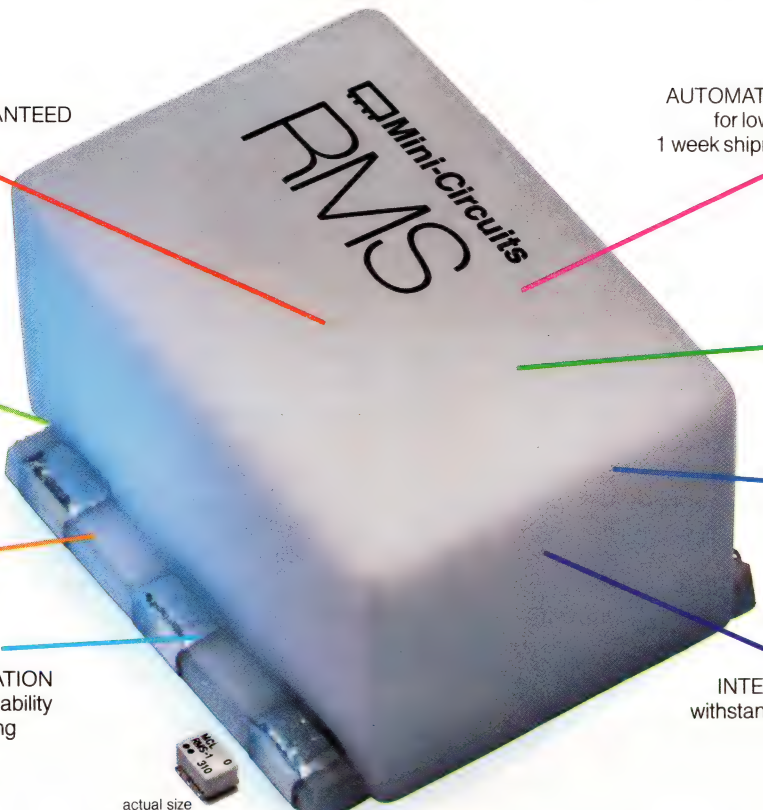

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using a high-frequency switch-mode controller. The Siliconix Si9145 controller uses switching frequencies as high as 2 MHz to provide voltage-mode PWM control to external switching elements. Efficiency in this configuration is a function of the magnetic losses and the external MOSFET's $r_{DS(on)}$.

Much of the impetus for 5-to-3.3V conversion comes from high-speed, current-hungry μPs. Two of the product families in **Table 2** target specific μPs. The Aries 57-S68060 linear regulator-in-a-socket allows you to upgrade your 5V 68040 system to accommodate a high-speed 68040V or 68060. And the Power Trends PT6501 8A switcher targets Pentium processors.

So far, the discussion has centered around converting 5 to 3.3V, and, in doing so, you can use either linear or switching regulators. In converting from a lower to a higher voltage, you need to use a switching regulator. These devices can produce 3, 3.3, or 5V from a single battery for powering ICs in pagers, personal digital assistants, palm computers, and other portable devices. Several of the ICs from Micro Linear in **Table 3** provide this up-conversion, with features such as 90% efficiency, shutdown isolation (disconnects battery when power is off) and ultralow (2-mV p-p) ripple.

Supervisory, control functions

In **Fig 2**, all the ICs have rudimentary control and supervisory functions. An enable or on pin functions as an on-off switch, putting the device into low-current standby (or sleep) mode when no demand for power exists. In addition, most regulator ICs have power-monitor pins, such as flag, which issue a signal when the output voltage falls out of regulation.

In μP-based systems, it's often wise to suspend digital processing when the power-supply line exhibits problems. A number of linear regulators provide a reset output that signals the system to cease logic operations. Upon initial power-up or upon the removal of a fault condition, it's usually not prudent to immediately initiate digital processing. A clock oscillator, for example, might require more than 100 msec to stabilize after power-up. For this reason, regulators with the reset function provide for a user-settable delay. With a ceramic capacitor, you can provide reset delays in the hundreds of milliseconds.

Another useful monitoring and supervisory function in many linear regulators is the watchdog utility. The regulator monitors the incoming signal from the μP's watchdog port. If the signal is at a steady low or high level, or if it's of the wrong frequency, the regulator generates a reset signal. A useful companion to the watchdog utility in a regulator is the wake-up function. The wake-up port in the regulator issues a signal to an I/O port to bring the μP out of sleep mode. The μP then signals its wake-up status to the regulator by issuing a watchdog signal.

Fig 3 shows a typical application of the reset, watchdog, and wake-up functions in a μP system. For the Cherry Semiconductor CS-8151 (**Table 3**), a single capacitor, C_{DELAY} in **Fig 3a**, determines the wake-up signal frequency, the wake-up delay time, and the reset pulse width. After power-up, the regulator issues a wake-up signal and waits for a watchdog signal from the μP (**b**). If the μP fails to send a watchdog signal within one wake-up period, the regulator issues a reset (**c**).

Modules and hybrids proliferate

As **Table 2** shows, modular and hybrid regulators are available in all sizes and shapes and offer power outputs from 1 to 280W. The most popular format for higher power converters is the 4.6×2.4-in. outline, which Vicor developed several years ago. Cutting the 4.6-in. length, several downsized models have recently appeared, with lengths of 3.5 and 3 in. and the half-size 2.3 in. The half-size VI-J00 Series from Vicor, for example, delivers (appropriately enough) 100W vs the 200W available from the company's full-size VI-200 Series.

Power output, efficiency, power density—these measures of modular and hybrid regulators' performance are of keen interest to system designers whose board space is limited. Impressive as some of the figures are for recent converters, however, be wary when interpreting them. For example, a "240W" converter might deliver that power for only one output voltage.

LOOKING AHEAD

The steady lowering of operating voltages in high-speed systems impacts power-supply development efforts in several ways. One formidable challenge is to achieve respectable efficiency figures in low-voltage dc/dc converters. This challenge is tough enough for 3.3V supplies; it becomes extremely difficult for the lower voltages that will inevitably come as IC geometries keep shrinking.

Diodes with low forward voltage and MOSFETs configured as synchronous rectifiers help to keep losses down and efficiency up. Germanium (Ge) diodes, for example, have much lower forward drop than do silicon rectifiers. Alas, reverse leakage vs temperature for Ge devices is abominable. Perhaps GaAs will be the next rectifier material of choice for makers of low-voltage supplies. In the meantime, power MOSFETs with extremely low on-resistance, such as the TrenchFET from Siliconix, can help keep losses down in sychronous-rectifier configurations.

Another challenge inherent in low-voltage systems is the need for enhanced supply-voltage accuracy. Traditional 5V systems can usually tolerate a sloppy 4.5-to-5.5V span. But that's not so with 3.3V ICs. Lower supply voltages bring reduced noise margins and correspondingly tight tolerances. So, power-supply designers must keep losses low and accuracy high.

One way to achieve a good efficiency-accuracy trade-off is to first convert the system bus voltage down with a switching circuit and then to use a low-dropout linear post-regulator to provide a clean and accurate output voltage. This technique borrows from the best of the switching and linear worlds, and it will probably be a popular configuration in future generations of low-voltage supplies.

ONBOARD REGULATORS

Table 4 shows the available output power for three manufacturers' 240W modules. For all three products, the output power for 3.3V-output products is less than 70% of that available from 15V-output models.

The reason for the compromised performance with lower output voltages is the finite forward voltage drops of rectifying elements. Whether in Schottky diodes or synchronous MOSFET switches, the nonzero forward voltage drops naturally become a larger proportion of the dc output voltage as the output voltage decreases. Until someone invents a perfect rectifying element, this fact of life will continue to limit the efficiency of low-voltage converters.

Caveat emptor: Before you get overimpressed by high power-density figures (usually expressed in watts per cubic inch), make sure you don't need a lot more cubic inches than the raw volume of the converter module. To meet certain emissions standards (notably, VDE), you must add input-filter modules or components to certain converters. To even determine the need for additional filtering, you have to confer with converter manufacturers, as many technical data sheets give little or no information about conducted emissions.

Another factor that can compromise power density is the need for heat sinking (see **box**, "Regulators need effective

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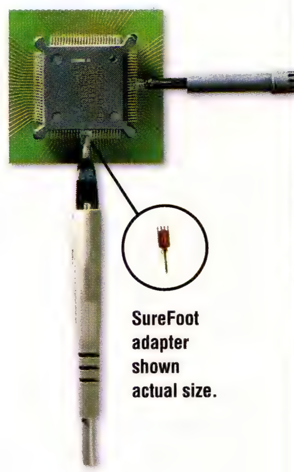

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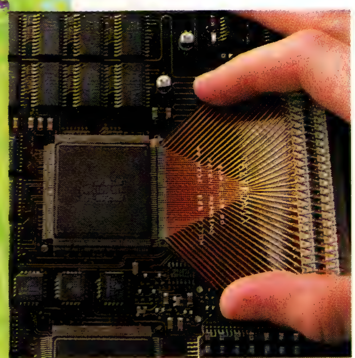

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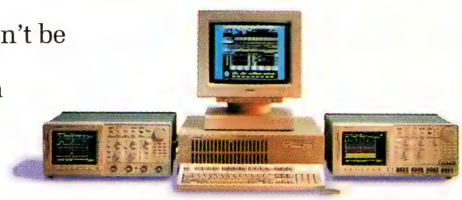

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ONBOARD REGULATORS

thermal management"). Most of the modular regulators have specs for maximum base-plate temperature, and heat-sink manufacturers offer standard products, design guides, and application assistance to help maintain that temperature. The same holds true for the monolithic regulators, all of which have specs for junction-to-case thermal resistance. The point here is that an "impressive" power density of X watts per cubic inch is of little interest if external components, modules, or cooling elements double or triple the final volume of the converter circuit.

Cooling a modular regulator, that is, keeping its base-plate temperature within limits, can be a complex undertaking. If you attach a heat sink to the base plate, you must decide upon the base-plate-to-sink interface medium: thermal grease or a thermal gasket. This medium fills surface voids or irregularities that can contribute to thermal resistance. Next, you should use the recommended torque for mounting bolts. Finally, you usually must provide forced air to remove the heat from the sink by convection.

Table 1 mentions redundancy. In fault-tolerant systems, you probably want to install redundant power converters. Several connections are possible, each with its pros and cons. The simplest is to connect two converters in a diode-OR arrangement. This method is not economical, because both converters must have the full load-current rating. Also, the series diodes waste power and degrade regulation.

Another method of supplying redundancy is a master-slave arrangement, in which one master converter controls one or more slaves, and all converters contribute equally to the load current. If one module fails, the remaining ones take up the slack. The drawback to this scheme is that the failure of the master converter causes the whole system to shut down.

Active current sharing, called N+1 or N+x redundancy, is the third way to configure a redundant system. In this method, the converters have a current-sharing pin that delivers a voltage proportional to the average output current supplied by the parallel-connected modules. Each module compares this level with its own output current and makes adjustments to its own output level to make the current-sharing equitable. An advantage of current sharing over using one converter is that you can use converters of lower power rating and thus lower cost while achieving the fault-tolerant benefits of redundancy.

TABLE 4—SWITCHING-REGULATOR P_{OUT} VS V_{OUT}

Output voltage	Abbott SM Series	Astec AM80A Series	Conversion Devices Power Pak Series
1.2	NA	72W	NA
2	80W	NA	NA
2.2	NA	132W	NA
3.3	132W	165W	165W
5	200W	200W	200W
12	240W	216W	216W
15	240W	240W	240W

NA=not available

In an extension of the current-sharing concept, Lambda Advanced Analog offers "stress-sharing" in its AFL Series of full-MIL-temperature 120W converters. These modules adjust current-sharing ratios according to case temperature to equalize stress among the parallel-connected converters.

In fault-tolerant systems using redundancy, you might require "hot-pluggability," the ability to remove and replace failed modules on the fly without shutting off system power. The problem with hot-plugging is the instantaneous load it imposes on the system power bus. The input stage of a power converter may contain a high-value filter capacitor connected across the input terminals. Under normal power-up conditions, this capacitor does not present a problem, because the ramp-up in system power-bus voltage allows the capacitor to charge normally. However, hot-plugging a cold power converter can create high inrush currents that could cause problems with the system power bus.

In **Ref 1**, Conversion Devices proposes the hot-pluggable input circuit in **Fig 4** to protect both the system power bus and the converter module. The R_1 divider network and C_1 provide the appropriate turn-on delay in Q_1. As Q_1 turns on, the input capacitor in the dc/dc converter charges at a controlled rate. The fuse limits input power in the case of catastrophic bus or module failures. Blocking diode D_1 provides reverse-voltage protection, and the avalanche zener diode, or MOV D_2, clamps the input to a safe level in the event of a system power-bus transient.

The task of configuring a power-distribution scheme is daunting. It involves many variables, some of which I only touch on here. The important thing is that you must consider power sources and voltage distribution early in the system-design effort, not as an afterthought. You must talk to regulator and converter manufacturers to make sure both published and unpublished product specs and features suit your requirements. EDN

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1. "Power-Pak Primer," Conversion Devices Inc, Brockton, MA.
2. "Linear Regulators with Microprocessor Control Functions," Application Note, Cherry Semiconductor Corp, East Greenwich, RI.

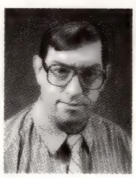

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TABLE 2—REPRESENTATIVE MODULAR AND HYBRID ONBOARD REGULATORS

Company	Model no.	Maximum output power	Input range (V dc)	Output voltages (V dc)
Abbott Electronics Circle No. 316	SM200S-270 SMH50/100	280 50 or 100	18 to 36, 175 to 400 18 to 36	2 to 28 2 to 28
Apex Microtechnology Circle No. 318	DHC2800 DB2800	6 22.5	11 to 50 15 to 50	3, 5, 12, 15 (single) ±12, 15 (dual) 5, 12, 15
Aries Electronics Circle No. 319	57-S68060	4	4.75 to 5.25	3.3
Astec Circle No. 320	AM80A	240	36 to 72, 180 to 400	1.2 to 15
AT&T Circle No. 321	TC050AB, TW050AB TC070AB, TW070AB	42 (peak spin-up) 60 (peak spin-up)	18 to 36, 36 to 72 18 to 36, 36 to 72	5, 12 5, 12
Calex Circle No. 323	SIP Series SD Series	1 17	4.5 to 5.5 4.5 to 6, 6.5 to 15	5, 12, 15 7, 14, 17 3.3, 5
Computer Products Circle No. 325	BXA3 Series BXA100 Series	3 100	9 to 18, 18 to 36, 36 to 74 36 to 75	3.3, 5, 12, 15, ±5, 12, 15 3.3, 5, 12, 15
Conversion Devices Circle No. 326	12000EH Series 24000S Series	120 240	36 to 72, 180 to 400 36 to 72, 180 to 400	3.3, 5, 12, 15 3.3, 5, 12, 15
Datel Circle No. 328	UWR (unipolar) BWR (bipolar) UNR-3.3/3000-D5 UNR-3.3/8000-D5 UNR-3.3/12000-D5 TWR Series	5 9.9 26.4 39.6 20	9 to 36, 18 to 72 4.5 to 5.5 4.5 to 5.5 4.5 to 5.5 9 to 36, 18 to 72	5, 12, 15 ±5, 12, 15 3.3 3.3 3.3 5 and ±12 or 15 (triple)
Ericsson Circle No. 330	PKG Series	60	38 to 75	3.3, 5
International Power Sources Circle No. 332	BT Series WT Series	3 5	5, 12, 24, 48 (±10%) 4.5 to 6, 9 to 18, 18 to 36, 36 to 72	5, 12, 15 (single) ±12, 15 (dual) 5, 12, 15 (single) ±12, 15 (dual)
Interpoint Circle No. 333	MK200	200	16 to 40, 18 to 40	5, 12, 15 (single or dual)
Lambda Advanced Analog Circle No. 335	AFL Series	120	28 or 270	5, 12, 15
Modular Devices Circle No. 341	3107R/3108R/3109R 3063 3064 3113 3114	20 30 50 20 80	16 to 50/86 to 158/200 to 335 8 to 50 8 to 50 8 to 50 8 to 50	3.3, 5, 12, 15, 28 (single) 5 and 12 or 15 (dual) 5 and ±5, 12, or 15 (triple) 3.3, 5, 12, 15, 28 (single) 5 and 12 or 15 (dual) 5 and ±5, 12, or 15 (triple) 3.3, 5, 12, 15, 28 (single) 5 and 12 or 15 (dual) and ±5, 12, or 15 (triple) 3.3, 5, 12, 15, 28 (single) 5 and 12 or 15 (dual) and ±5, 12, or 15 (triple) 3.3, 5, 12, 15, 28 (single) 5 and 12 or 15 (dual) and ±12 or 15 (triple)
Pico Electronics Circle No. 344	AV Series LPD Series	1.25 75	5, 12, 24, 28 200 to 380	100 to 500 3.3 to 100 (single) 5 to 48 (dual)
Power Convertibles Circle No. 345	VKP60R WP20R	60 20	36 to 72 18 to 36, 36 to 72	3.3, 5, 12, 15, 24, 28 5, 8, 12 (single) ±12, 15 (dual)
Power Trends Circle No. 346	PT6501 PT6502	26.4 20	4.5 to 6 6 max	3.3 1.5 to 2.5 (adjustable)
Vicor Circle No. 354	VI-J00 Series	100	10 to 375 (10 ranges)	2, 3.3, 5, 12, 15, 24, 28, 48
Wall Industries Circle No. 355	HD Series KR Series	150 6	18 to 36, 20 to 60, 36 to 72 9 to 18, 18 to 36, 36 to 72	5 to 48 (single) ±5 to 24 (dual) 5 and ±12 or 15 (triple) 5 to 15 (single or dual)

Size (l×w×h (in.))	Power density (W/in.^{3})	Price	Comments
4.2×2.4×0.5 2.3×2.4×0.5	50 18 or 36	\$600 (1000) \$450 (1000)	SM modules use hermetic, MIL-grade ICs; meets MIL-STD-704D and -810E.
1×1×0.35	17	\$225.50 (100)	Remote output-voltage sense; case temperature to 125°C.
1.6×1.63×0.495	22.5	\$298 (100)	Remote shutdown pin; case temperature to 125°C.
Built into 68040V or 68060 socket	NA	\$195 (100)	Optional 3.6V output for higher μP speed.
4.6×2.4×0.5	43	\$162 (1000)	Has isolated, low-voltage secondary-side controls.
3.5×2×0.625 3.5×2×0.625	10 (peak) 14 (peak)	\$35 (1000) \$50 (1000)	TC, TW Series designed for disk-drive power.
0.77×0.24×0.38	14	\$9 (1000)	7, 14, 17V units designed to drive three-terminal regulators.
2×0.5×0.75	23	\$38 (1000)	Remote on/off control minimizes current drain.
1.25×0.8×0.5	6	\$20 (1000)	UL, IEC, VDE, EN, CSA safety approvals in process for all BXA models. All models characterized for VDE, EN, FCC, or CISPR conducted-emissions standards. 10, 15, 30, and 75 models also available in BXA Series.
3.5×2.4×0.5	24	\$100 (1000)	
2.3×2.4×0.5 4.6×2.4×0.5	43 43	\$122.50 (100) \$148 (100)	Fixed 500-kHz operation; UL, CSA, VDE safety approvals. Accurate current sharing in parallel connection.
1×1×0.45	11	\$47 (100)	Maintains standard pinout of 2×2-in. packages.
1×1×0.45 2×1×0.45 2×2×0.45 2×2×0.45	22 29 22 11	\$44 (100) \$53 (100) \$58 (100) \$74 (100)	UNR models have ±1% output accuracy, efficiencies to 90%. UL, CSA, IEC safety approvals pending; power sharing architecture provides any combination of 5V and bipolar power to 20W.
2.94×2.41×0.43	20	\$61 (500)	Designed for forced-air convection cooling; needs no heat sink; Meets EN and UL telecomm safety standards.
1.25×0.8×0.4	7.5	\$10 (1000)	500V input-output isolation.
1.25×0.8×0.4	12.5	\$25 (1000)	π-network input filter.
2.4×2.28×0.45	81	\$590 (1000)	Fixed 1.2-MHz switching rate.
2.5×1.5×0.368	87	\$720 (100)	Full MIL temperature range.
2.12×1.12×0.495	17	\$915/985/985 (10)	Rad-hardened; EMI filtering to MIL-STD-461C.
2.15×1.34×0.495	21	\$1204 (10)	All models feature EMI filtering to MIL-STD-461C.
2.7×2.6×0.495	14	\$1528 (10)	
2.12×1.12×0.495	17	\$915 (10)	
2.7×2.6×0.495	23	\$1757 (10)	
0.5×0.5×0.4 2.4×2.3×0.5	12.5 27	\$80.12 (units) \$104 (units)	100-MΩ isolation at 1000V. Remote-shutdown pin.
2.15×2.05×0.46 2×2×0.4	30 12.5	\$93 (500) \$51.11 (1000)	100°C base-plate temperature. π-network input filter.
1.64×0.36×1.16 1.64×0.36×1.16	40 30	\$25 (1000) \$25 (1000)	90% efficient at 3A output. Designed for bus terminations.
2.28×2.4×0.5	37	\$100 (units)	BABT-, UL-, CSA-, IEC-, BSI-approved.
4.6×2.4×1	14	\$122.20 (1000) \$137.35 (1000) \$146.95 (1000)	Active current sharing.
1×2×0.38	8	\$53 (1000)	Low-ESR output capacitor.

TABLE 3—REPRESENTATIVE MONOLITHIC ONBOARD REGULATORS

Company	Model no.	Type	Maximum output current	Input range (V dc)
Allegro Microsystems Circle No. 317	A8183SLU	Low-dropout	150 mA	4 to 8
	A8184SLU	Low-dropout	150 mA	4 to 8
	A8186SLU	Low-dropout	150 mA	4 to 8
	A8187SLU	Low-dropout	150 mA	4 to 8
Burr-Brown Circle No. 322	REG1117-2.85	Low-dropout	800 mA	4.05 to 10
	REG1117-3	Low-dropout	800 mA	4.5 to 10
	REG1117-3.3	Low-dropout	800 mA	4.8 to 10
	REG1117-5	Low-dropout	800 mA	6.5 to 10
	REG1117	Low-dropout	800 mA	1.5 to 13.75
Cherry Semiconductor Circle No. 324	CS-8121	Low-dropout	1A	7 to 26
	CS-8125	Low-dropout	500 mA	6 to 26
	CS-8129	Low-dropout	750 mA	6 to 26
	CS-8135	Low-dropout	750 mA	6 to 26
	CS-8140/8141	Low-dropout	500 mA	7 to 26
	CS-8145	Low-dropout	750 mA	11 to 16
	CS-8147	Low-dropout	500 mA	13 to 26
	CS-8151	Linear	100 mA	6 to 26
	CS-8155	Low-dropout	750 mA	13 to 26
	CS-8156	Low-dropout	750 mA	13 to 16
	CS-8165	Low-dropout	750 mA	13 to 26
Harris Semiconductor Circle No. 331	HIP5060	Switching	10A	27 to 45
	HIP5062	Switching	5A, 5A (dual)	26 to 42
	HIP5063	Switching	10A	10 to 45
Linear Technology Circle No. 337	LTC1314	Switching	120 mA	5 and 12
	LTC1315	Switching	120 mA	5 and 12
	LT1120A	Low-dropout	125 mA	4.5 to 36
	LTC1159	Switching	Configurable	4 to 40
	LT1584	Low-dropout	7A	4.75 to 7
	LT1585	Low-dropout	4A	4.75 to 7
	LT1587	Low-dropout	3A	4.75 to 7
Maxim Integrated Products Circle No. 338	MAX603/604	Low-dropout	500 mA	4.3 or 6 to 11.5
	MAX687/688	Low-dropout	10-mA base drive	4.3 or 6 to 11.5
	MAX689	Low-dropout	10-mA base drive	4.3 or 6 to 11.5
	MAX882/884	Low-dropout	200 mA	4.3 to 11.5
	MAX883	Low-dropout	200 mA	6 to 11.5
Micrel Semiconductor Circle No. 339	MIC2920A	Low-dropout	400 mA	V_{OUT}+450 mV min
	MIC2937A	Low-dropout	750 mA	V_{OUT}+370 mV min
	MIC2940A	Low-dropout	1.25A	V_{OUT}+300 mV min
	MIC29150	Low-dropout	1.5A	V_{OUT}+450 mV min
	MIC29300	Low-dropout	3A	V_{OUT}+450 mV min
	MIC29500	Low-dropout	5A	V_{OUT}+450 mV min
	MIC29750	Low-dropout	7.5A	V_{OUT}+450 mV min
	MIC5156	Switching	Configurable	3 to 36
	MIC5157	Switching	Configurable	3 to 36
	MIC5158	Switching	Configurable	3 to 36
Micro Linear Circle No. 340	ML4861	Switching	300 mA	1 to 5.5
	ML4862	Switching	Configurable	5.4 to 24
	ML4875	Switching	410 mA	1 to 4.5
	ML4890	Switching	100 mA	0.9 to V_{OUT}–0.2V
National Semiconductor Circle No. 342	LP2952	Low-dropout	250 mA	V_{OUT}+0.47V to 30
	LP2953	Low-dropout	250 mA	V_{OUT}+0.47V to 30
	LP2980	Low-dropout	50 mA	V_{OUT}+0.225V to 16
Siliconix Circle No. 351	Si9145	Switching	200-mA gate drive	2.7 to 7
Unitrode Circle No. 353	UCC383T-3	Low-dropout	3A	V_{OUT}+1 to 9
	UCC383T-5	Low-dropout	3A	V_{OUT}+0.6 to 9
	UCC383T-ADJ	Low-dropout	3A	V_{OUT}+0.6

Output voltage (V dc)	Package(s)	Price	Features
3	Six-lead SO	$0.82 (1000)	Enable, uses PMOS pass element
3	Four-lead SO	$0.48 (1000)	A8183SLU without enable pin
3.3	Six-lead SO	$0.82 (1000)	Enable, uses PMOS pass element
3.3	Four-lead SO	$0.48 (1000)	A8186SLU without enable pin
2.85	SOT-23	$1.50 (10,000)	Alternate source for Linear
3	SOT-23	$1.50 (10,000)	Technology LT1117
3.3	SOT-23	$1.50 (10,000)	
5	SOT-23	$1.50 (10,000)	
Adjustable	SOT-23	$1.50 (10,000)	
5	TO-220	$1.13 (10,000)	Reset, enable
5	TO-220	$1.11 (10,000)	Delayed reset
5	TO-220, 16-lead SO	$0.94 (10,000)	Delayed reset
5 and 5 (dual)	TO-220	$1.11 (10,000)	Reset, enable
5	TO-220, 14-pin DIP,		
	24-lead SO	$1.75/1.84 (5000)	Reset, enable, watchdog
5 and 10 (dual)	TO-220	$1.11 (10,000)	Enable
5 and 10 (dual)	TO-220	$1.18 (10,000)	Enable
5	TO-220, 16-pin DIP,		
	16-lead SO	$1.56 (10,000)	Reset, watchdog, wake-up
5 and 12 (dual)	TO-220	$1.11 (10,000)	Enable
5 and 12 (dual)	TO-220	$1.18 (10,000)	Enable
5 and 8 (dual)	TO-220	$1.11 (10,000)	Enable
Configurable	Die form	$6.18 (1000)	All models feature current-
Configurable	Die form	$7.33 (1000)	mode control, 1-MHz switching
Configurable	Die form	$4.33 (1000)	
3.3, 5, 12	14-lead SO	$2.26 (1000)	Controls PCMCIA 2.0 slot
3.3, 5, 12	24-lead SO	$3.23 (1000)	Dual version of LTC1314
5	Eight-pin DIP, eight-lead SO	$2.60 (100)	Shutdown, on-chip comparator
3.3, 5	16- or 20-lead SO	$4.70 (1000)	Drives external MOSFETs
3.3, 3.38, 3.45, 3.6	TO-220	$5.82 (1000)	LT1584/1585/1587 available in
3.3, 3.38, 3.45, 3.6	TO-220 (through-hole		adjustable versions
	or surface-mount)	$3.72 (1000)	
3.3, 3.38, 3.45, 3.6	TO-220 (through-hole or	$3.22 (1000)	
	surface-mount)		
3.3, 5	Eight-pin DIP, eight-lead SO	$1.68 (1000)	Shutdown, power-fail pins
3.3	Eight-pin DIP, eight-lead SO	$1.60 (1000)	Drives external pnp transistor
3	Eight-pin DIP, eight-lead SO	$1.60 (1000)	Drives external pnp transistor
3.3	Eight-pin DIP, eight-lead SO	$1.45 (1000)	Shutdown, on-chip comparato
5		$1.45 (1000)	
3.3, 5, 12	Eight-pin DIP, eight-lead SO,	$1.14 (100)	Shutdown, error flag
	TO-220, SOT-223		
3.3, 5, 12	TO-220, TO-263	$1.55 (100)	Shutdown, error flag
3.3, 5, 12	TO-3, TO-220, TO-263	$1.65 (100)	Shutdown, error flag
3.3, 5, 12	TO-220, TO-263	$1.93 (100)	Shutdown, error flag
3.3, 5, 12	TO-220, TO-263	$2.64 (100)	Shutdown, error flag
3.3, 5, 12	TO-3, TO-220	$4.50 (100)	Shutdown, error flag
3.3, 5, 12	TO-3, TO-247	$7.50 (100)	Shutdown, error flag
3.3, 5	Eight-pin DIP, eight-lead SO	$1.38 (1000)	Drives external MOSFET
3.3, 5, 12	14-pin DIP, 14-lead SO	$1.54 (1000)	Drives external MOSFET; has
			charge pump for gate drive
Adjustable	14-pin DIP, 14-lead SO	$1.54 (1000)	Adjustable version of MIC5157
3.3, 5, 6	Eight-lead SO	$1.95 (1000)	Undervoltage lockout; uses external L, C
3.3 and 5	32-lead SO	$5.95 (1000)	Uses four external MOSFETs; contains
			5 and 12V linear regulators
3.3, 5	Eight-lead SO	$2.50 (1000)	Undervoltage lockout;
			uses external L, C
3, 3.3, 5	Eight-lead SO	$2.95 (1000)	Uses external L+2C
3.3	14-pin DIP, 16-lead SO	$2 (1000)	Shutdown, error flag
3.3	16-pin DIP, 16-lead SO	$2.30 (1000)	LP2952 with auxiliary comparator
3, 3.3, 5	Five-lead SO	$0.77 (1000)	375-µA ground current at full load
Configurable	16-lead SO	$1.64 (100,000)	Enable, standby; uses external
			MOSFET(s); switch rate to 2 MHz
3.3	TO-220, TO-263	$3.38 (1000)	BiCMOS; contains MOSFET pass
5	TO-220, TO-263	$3.38 (1000)	element, time-delayed current limit
Adjustable	TO-220, TO-263	$3.72 (1000)	


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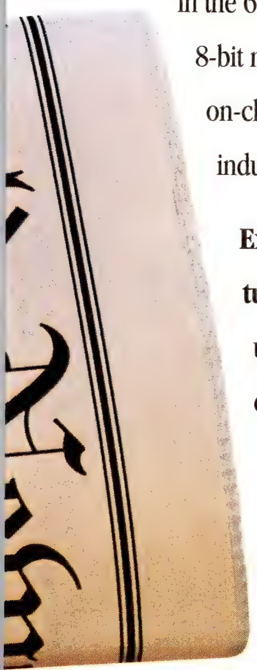

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HIGH-DENSITY FLASH MEMORY

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Most designers avoid high-density flash simply because they are unfamiliar with what type to use—and where to use it. As densities increase, prices drop below the cost of DRAM, and manufacturers enhance performance, flash memory is gaining momentum. It just may become an integral part of your next system design.

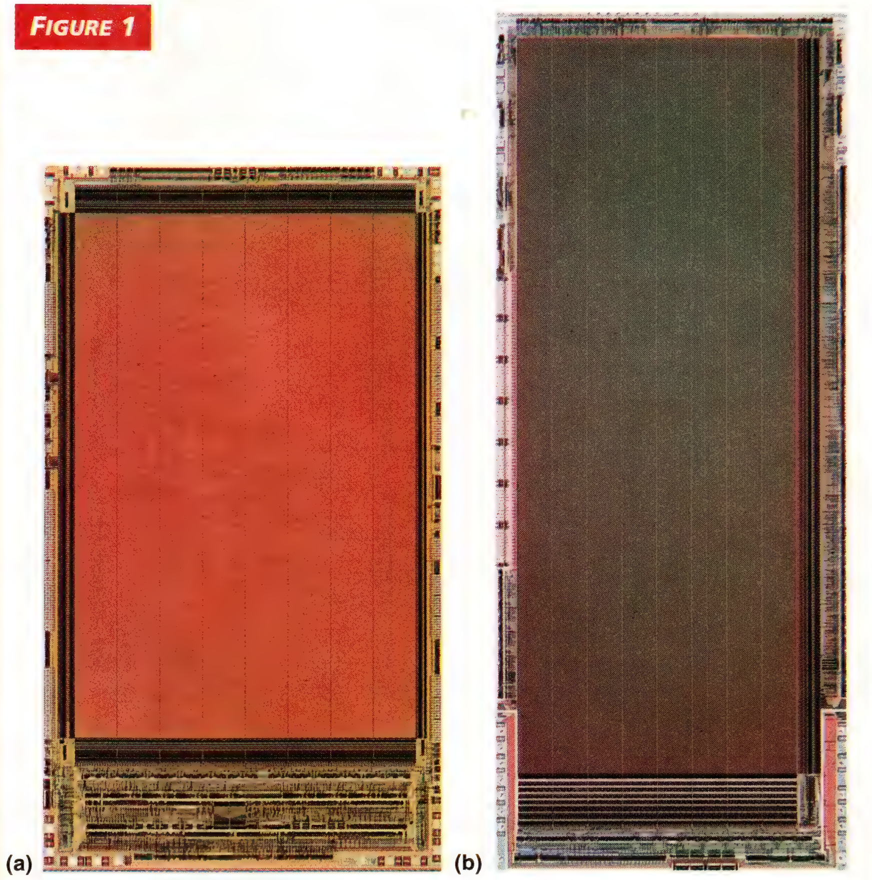
MARKUS LEVY, TECHNICAL EDITOR

Six years ago, flash memory was virtually unheard of in the electronics industry. Today, designers are taking advantage of flash's multiple useful characteristics, including nonvolatility, the ability to update in circuit, low power consumption, and high density. There is a downside to flash, however, and its shortcomings continue to impede widespread growth. Flash faults include high cost, slow read and write speeds, nonstandardized interfaces, and widespread lack of availability.

Manufacturers are striving to eliminate or to reduce the most obvious shortcomings of flash, beginning with the debut of a 16-Mbit generation. Flash prices have just dropped below the cost of DRAMs, second sources are evolving, manufacturers are developing de facto standards, and the technology is approaching optimal performance levels.

Designers have access to a wide assortment of flash-memory device types. Densities range from 256 kbits to 32 Mbits (**Fig 1**). Erase-block sizes range from 512 bytes to 128 kbytes. Power-supply voltages are either 3.3 or 5V; write/erase voltages are 3.3, 5, or 12V. Some flash devices are symmetrically blocked, and others have asymmetric erase blocks. On the other hand, bulk-erase flash devices lack blocking alto-

FIGURE 1



Due to continually shrinking design rules, Samsung's 32-Mbyte NAND flash (a) is approximately 6% smaller than the previous-generation 16-Mbyte device (b).

gether. But, of all flash-device types, In-Stat predicts that high-density devices will provide the most interesting story: High-density flash will experience the most significant market-share growth in upcoming years. (Devices 2 Mbits and below are on the decline.)

High-density devices contain several flash architectures. The differences between NOR, NAND, AND, divided-bit-line NOR (DINOR), and triple-poly architectures center primarily around the method of erase and write and the organization of the transistors within the device. Designers generally can afford to overlook the details of these architectural differences in order to concentrate on the features or capabilities associated with a specific architecture.

NOR FLASH

Within NOR flash, any byte is randomly accessible from a read and write perspective (with the exception that a byte cannot be rewritten unless its associated block is erased). This aspect of NOR flash suits it particularly well for code storage and execute-in-place (XIP) applications, which require high-speed random access. Access times range from 65 to 170 nsec. Intel's 28F016XS, a synchronous flash memory with a three-stage pipeline, broke the speed record with access times to 30 nsec (**Fig 2**). This move translates to zero-wait-state performance at 33 MHz, with burst lengths up to the full 2 Mbytes.

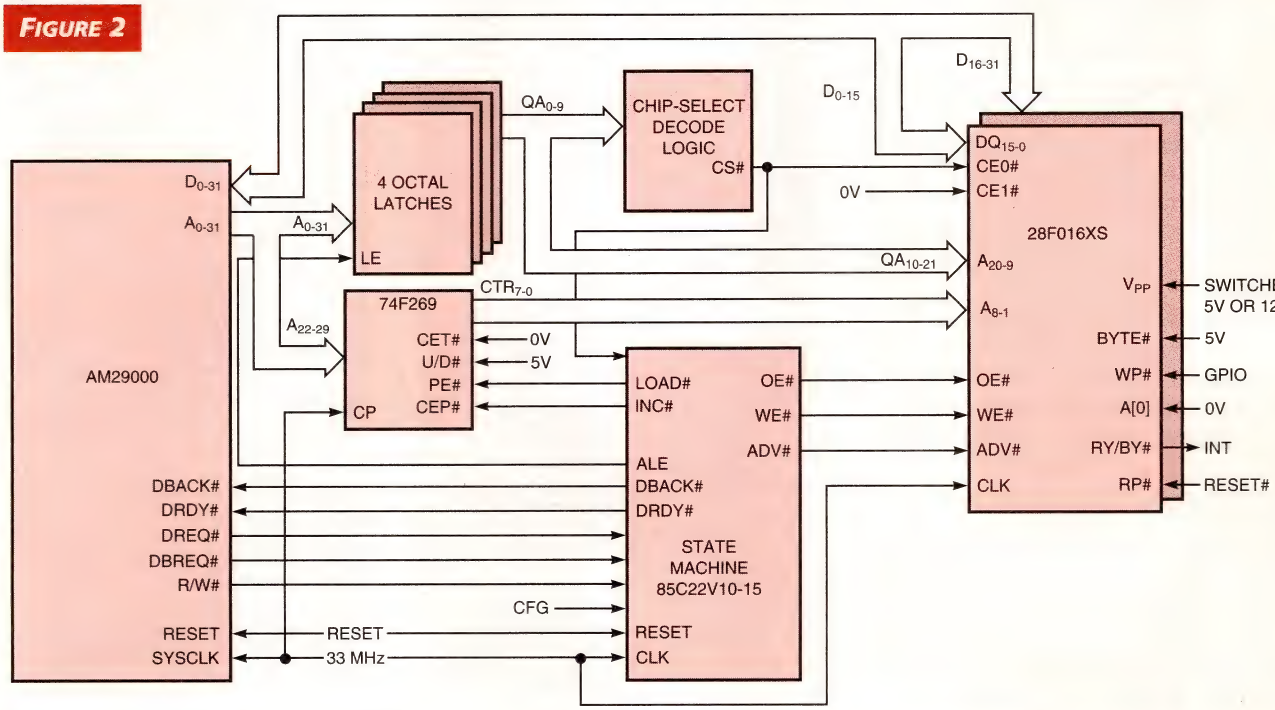
Traditionally, NOR flash has been associated with large, 64-kbyte erase blocks and long erase times of 1 to 2 sec. Although the large block size minimizes the erase granularity, it also minimizes the overhead control circuitry needed to access the array; this, in turn, minimizes the die size, which allows a lower cost structure. Hitachi's HN28-F1600 16-Mbit device, with 512-byte sectors (or blocks), breaks the mold on erase sector size and erase time for NOR flash. Each 512-byte sector in the HN28F1600 erases in 10 msec (typ), but the sectors can be configured into larger block sizes of up to 32 contiguous sectors and erased in 15 msec (typ).

Compared with RAM, NOR-flash write time is several orders of magnitude slower, typically 7 to 10 μsec/byte. Intel's 16-Mbit flash devices have two integrated 256-byte RAM buffers for increasing the burst-write-transfer rate. Once data is in the buffers, the system gives the flash device the command to transfer the data

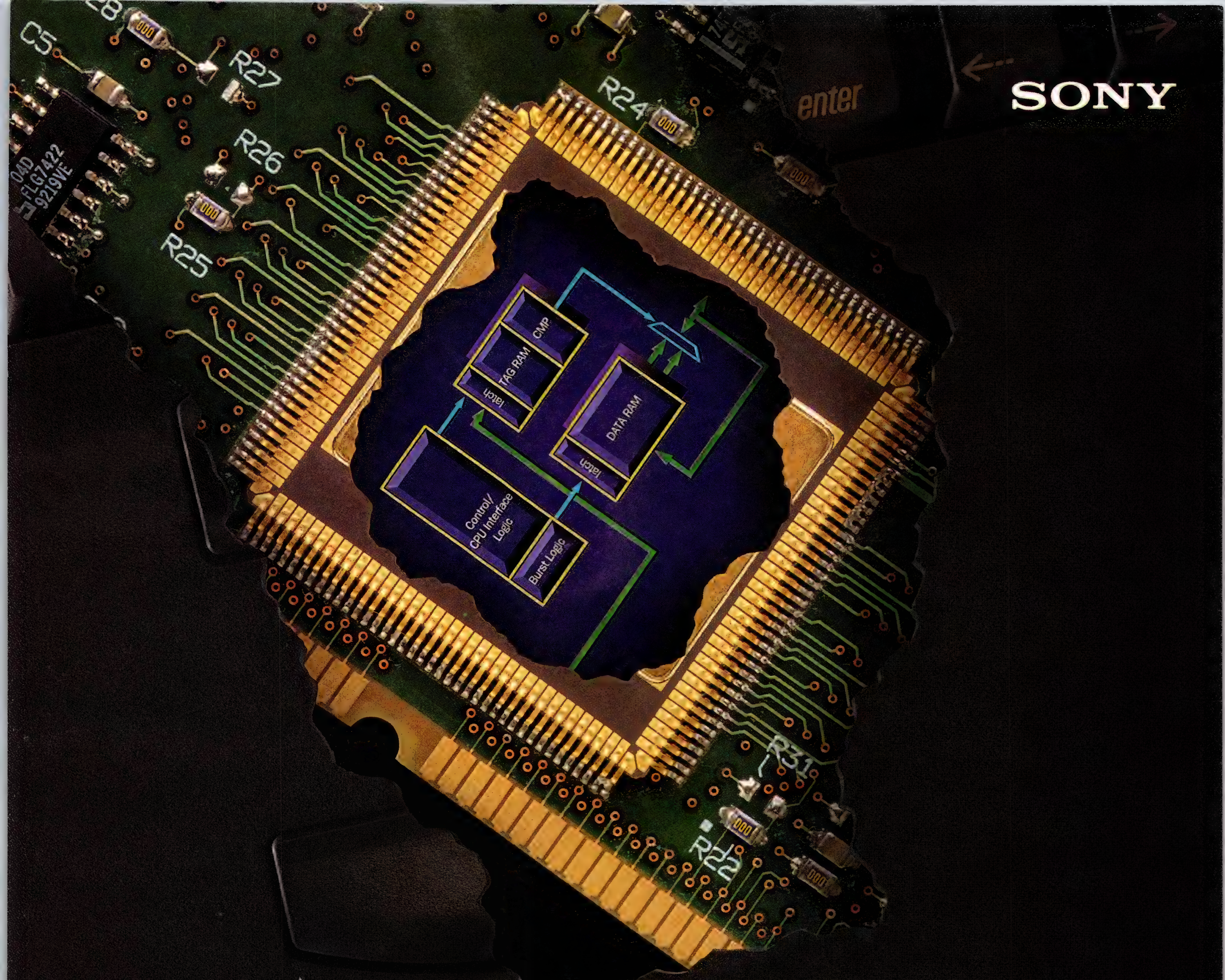
IN PCs, DISK DRIVES CONTINUE TO OUTPACE FLASH

For several years to come, flash-memory solid-state drives (SSDs) will struggle to compete with disk drives used in the PC. Although flash densities are increasing rapidly, to keep up with the growing size of PC applications, so, too, are disk-drive densities. SSDs compete against products such as the SQ1080 from Syquest (Fremont, CA, (800) 245-2278). This 80-Mbyte hard-disk drive, in a PCMCIA form factor, is unique in that you store its data on removable cartridges, analogous to storage on floppy disks. You can buy the drive (motors, head, etc) and one cartridge for approximately \$500; additional 80-Mbyte cartridges cost \$80. An SSD of the same density would have an end-user price tag of approximately \$4000.

FIGURE 2



Designers can integrate Intel's 28F016XS with minimal logic to burst-capable processors, such as the i960 or Am29000. The Am29000 interface here requires latches to retain the starting address of the burst sequence.



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into the flash array at a rate of 3 μsec/byte, approximately twice as fast as writing 1 byte at a time. Similar to Intel's 16-Mbit flash, Hitachi's HN28F1600 writes 1 byte at a time, but the device also has an 8-byte page for increased write performance. Specifically, the Hitachi flash typically writes 1 byte in 10 μsec or an 8-byte page in 20 μsec.

NAND FLASH

NAND flash is structured such that the system reads or writes on a page basis, where a page equals 264 bytes of SRAM (256 plus 8 bytes for error correction). The 32-Mbit device has a 528-byte page (512 plus 16 bytes for error correction). The system accesses data sequentially within those pages. NAND flash's system interface consists of I/O pins for both address and data input and output as well as command inputs. After the system provides a command to read data from the device, internal circuitry transfers data from the flash array into the page. Once the data is in the page, it streams out of the device at an 80-nsec/byte rate (typ). However,

TABLE 1—REPRESENTATIVE HIGH-DENSITY FLASH-MEMORY DEVICES (16MBITS AND ABOVE)

Vendor	Device (in Mbits)	Technology	Bus width	Supply voltage	Programming voltage	Block-erase time/size
AMD Circle No. 301	Am29F016 (16)	NOR	x8	5	NA	1 sec/64 kbytes
Hitachi Circle No. 302	Unnamed (32)	AND	x8	3	NA	NI
	HN28F1600 (16)	NOR	x8,16	5	12	10 msec/ 512 bytes
Intel Circle No. 303	28F016SA (16); 28F032SA (32)	NOR	x8,16	3 or 5	12	0.6 sec/64 kbytes
	28F016SV (16)	NOR	x8,16	3 or 5	5 or 12	0.6 sec/64 kbytes
	28F016XD[2] (16)	NOR	x16	3 or 5	5 or 12	1.2 sec/128 kbytes
	28F016XS (16)	NOR	x8,16	3 or 5	5 or 12	1.2 sec/128 kbytes
Mitsubishi Circle No. 305	M5M28F016 (16)	NOR	x8	3 or 5	12	2 sec/64 kbytes
National Semiconductor Circle No. 307	Nm29N16	NAND	x8	5	NA	6 msec/4 kbyte
Samsung Circle No. 309	KM2916000 (16)	NAND	x8	5	NA	6 msec/4 kbytes
	KM2932000 (32)	NAND	x8	5	NA	5 msec/8 kbytes
SGS-Thomson Circle No. 310	M28F161 (16); M29F161 (16)	NOR	x8	3;5	12[3]	NI
Sundisk Circle No. 311	No name (16)	Triple-poly	x2	5	5 or 12	1 msec/512 bytes
	No name (32)	Triple-poly	x2	3 or 5	3 or 5	1 msec/512 bytes
Toshiba Circle No. 312	TL5816 (16)	NAND	x8	5	NA	12 msec/4 kbytes

Notes:
1. NA=Not applicable; NI=No information available.
2. Micron is designing Intel-compatible devices (due in 1996), one with a DRAM interface with extended-data-out read (30-nsec read access) and another that is Intel 28F008SA-compatible.
3. M29F161 is AMD-compatible; therefore, it's single-voltage.

the initial loading of the page takes approximately 25 µsec, which wreaks havoc on NAND flash's random read access. NAND flash is not optimized for code storage or XIP applications.

Similar to the RAM buffers on Intel's 16-Mbit device, the NAND flash's page allows the system to perform burst writes to the device. Note that after the 264- or 528-byte page fills, NAND flash may require up to 5 msec to transfer the page's contents into the flash array.

NAND flash has small erase blocks and fast erase times. The 16- and 32-Mbit devices have a maximum of 512 erase blocks of 4 and 8 kbytes, respectively. NAND-flash manufacturers ship perfect and imperfect devices, each with a different price structure. Perfect devices have 100% functional blocks; imperfect devices have up to 2% bad blocks, which increases yields. After the manufacturer tests the flash device, 00H is programmed somewhere within the bad blocks. After installing these devices, system software identifies (and maps) the bad blocks by scanning for

Byte program time	Page program time and size	Read-access time	Special features	Availability	Cost (qty)
8 µsec	NA	90 nsec	Negative gate erase, single voltage, write protection.	Now	$60 (1000)
NI	NI	120 nsec (random), 50 nsec (sequential)	Detailed specs available this year.	Q4	NI
10 µsec	20 µsec/8 bytes	120 nsec		Q1	$65 (10,000)
6 µsec	1.2 msec/256 bytes	70 nsec	Page buffers, individual block locking, deep power-down mode, command queuing.	Now	$41; $102 (10,000)
6 µsec	1 msec/256 bytes	65	Same as above plus SmartVoltage.	Now	$49 (10,000)
6 µsec	1 msec/256 bytes	65	Same as above plus DRAM interface.	Now	$49 (10,000)
6 µsec	1 msec/256 bytes	30	Same as above plus synchronous pipelined interface.	Now	$55 (10,000)
15 µsec	NA	100 nsec		Q1	$60 (1000)
NA	400 µsec/264 bytes	25 µsec/ 80 nsec	Although compatible with Toshiba's and Samsung's NAND flash, prices and specs may vary.	Q4	$52 (1000)
NA	300 µsec/256 bytes	20 µsec/ 80 nsec	Although compatible with National's and Toshiba's NAND flash, specs and pricing vary.	Now	$49 (5000)
NA	200 µsec/512 bytes	10 µsec/ 50 nsec		Samples	NI
10 µsec	NA	100 nsec 90 nsec		Q2 of 1996	NI
NA	6 µsec/32 bytes burst	3 Mbytes/sec	System level only, no discrete components.	Now	$100 1.8-Mbyte drive. (10,000)
NA	6 µsec/32 bytes burst	3 Mbytes/sec	System level only, no discrete components.	Production in Q2	$75 2-Mbyte drive. (1000)
NA	300 to 1000 µsec/ 265 bytes	25 µsec/ 80 nsec	Although compatible with National's and Samsung's NAND flash, specs and pricing may vary.	Now	$35 (1000)

HIGH-DENSITY FLASH MEMORY

00H. This process is analogous to bad sectors on a disk drive.

The erase time (and current consumption) on NAND devices does not vary considerably between a single block and an entire chip erase. A single block erases in a maximum of 100 msec (6 msec is typical); simultaneous, multiblock erases (up to the entire chip) take a maximum of 130 msec. Compare this with the maximum chip-erase time of 19 sec (1 sec typ) that 16-Mbit NOR devices require—they must erase all blocks sequentially (with the exception of Hitachi's HN28F1600).

AND FLASH

The AND flash, primarily driven by Hitachi, is a new cell structure that incorporates characteristics of NAND and NOR architectures. The first commercially available AND device contains a 32-Mbit flash array. Some of the AND flash characteristics include 512-byte erase blocks and random- and sequential-access modes. In random mode, you can access data in 120 nsec. Sequential mode has a 1-μsec hit for the first access while a page buffer fills, but then subsequent accesses can stream at 50 nsec/byte.

DINOR FLASH

The basic cell structure of DINOR flash looks much like a NOR flash cell. The major differences between the two architectures are in the erase and write methods, as well as the cell arrangement. In short, NOR flash uses a main metal line, and DINOR flash has a polysilicon sub-bit line to reduce contact area, ultimately reducing the die size by 25% and allowing faster access. As with other flash devices, the DINOR device includes a 256-byte buffer to increase burst-write performance. The DINOR flash also allows low-current write and erase, which makes it practical to integrate an on-chip charge pump to generate internal high voltages from 3.3V. Hitachi will introduce the first DINOR (16-Mbit) flash device in the third quarter.

TRIPLE-POLY FLASH

The triple-poly architecture, which Sundisk uses, produces a die with a very dense array. The Sundisk flash device writes 32 bytes in parallel (10 μsec) because the flash cells program in relatively low channel currents. Erase sector size is 512 bytes, in addition to 10% overhead for memory management and error checking and correction. Typical erase time is 1 msec, and a sector-tagging feature allows multiple sectors to erase in parallel. Sundisk is unusual in that it builds flash devices solely for its own use in its ATA drives. (Oki Semiconductor is doing the same.) Because Sundisk's flash devices are buried within an ATA drive, designers can relocate repetitive on-chip circuitry on a single off-chip controller, reducing die size further. To increase yields, Sundisk uses devices with known defects, but the ATA drive's internal logic maps out the bad blocks.

High-density flash applications

Solid-state drives (SSDs) and DRAM replacement promise to be the biggest consumers of high-density flash. Many flash manufacturers bet on personal digital assistants (PDAs) to become the main consumers of SSDs. Unfortunately, PDAs haven't yet reached their anticipated popularity. Currently, embedded applications are the primary users of flash-memory SSDs.

Applications such as digital-answering-machine and voice-mail audio storage; cameras, fax machines, and scanner image storage; and video games are becoming significant consumers of high-density flash. PCMCIA cards, used in an unlimited number of applications, are also significant consumers of high-density flash.

SSDs represent a large potential market for high-density flash. Many manufacturers promote their specific flash technology as a viable candidate for this application. Technically, all flash architectures work in SSDs, but designers still have to wrestle with the file-management algorithms that make the SSDs work. First, it's important to

MANUFACTURERS OF HIGH-DENSITY FLASH MEMORIES

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define an SSD, which predominantly refers to a file-storage device with an IDE or PCMCIA-ATA interface to the host system (although you can use other interfaces, such as SCSI). The main function of the nonflash components (hardware and software) within an SSD is to translate the system's requests for file accesses into a flash-compatible format. The idea here is that the system still thinks it's communicating with a disk drive.

Although many ready-made SSDs are available, Cirrus Logic (Fremont, CA, (510) 226-2123)) provides flash controller chips you can use to develop your own SSD directly on your system's motherboard or in a PCMCIA-ATA form factor (**Fig 3**). Cirrus Logic's controller, the CL-ST1000, supports one of Hitachi's 16-Mbit flash components. (Cirrus plans to introduce controllers that support other flash devices.) The CL-ST1000, which costs $22 (1000), comes with a reference design that includes schematics, board layouts, and firmware. To build an SSD larger than 2 Mbytes, you must also buy Cirrus Logic's CL-ST2000 Space Manager (an additional $18 (1000)). Alternatively, National Semiconductor plans to provide software and reference designs to help OEMs develop their own SSDs.

Some SSDs consist solely of a flash-memory array, in the form of a PCMCIA card, or as discrete components with a custom interface to the host. The host CPU, as opposed to a dedicated controller, handles all file management using device drivers. Companies such as M-Systems (Santa Clara, CA, (408) 654-5820) have developed flash-device drivers for NAND or NOR flash.

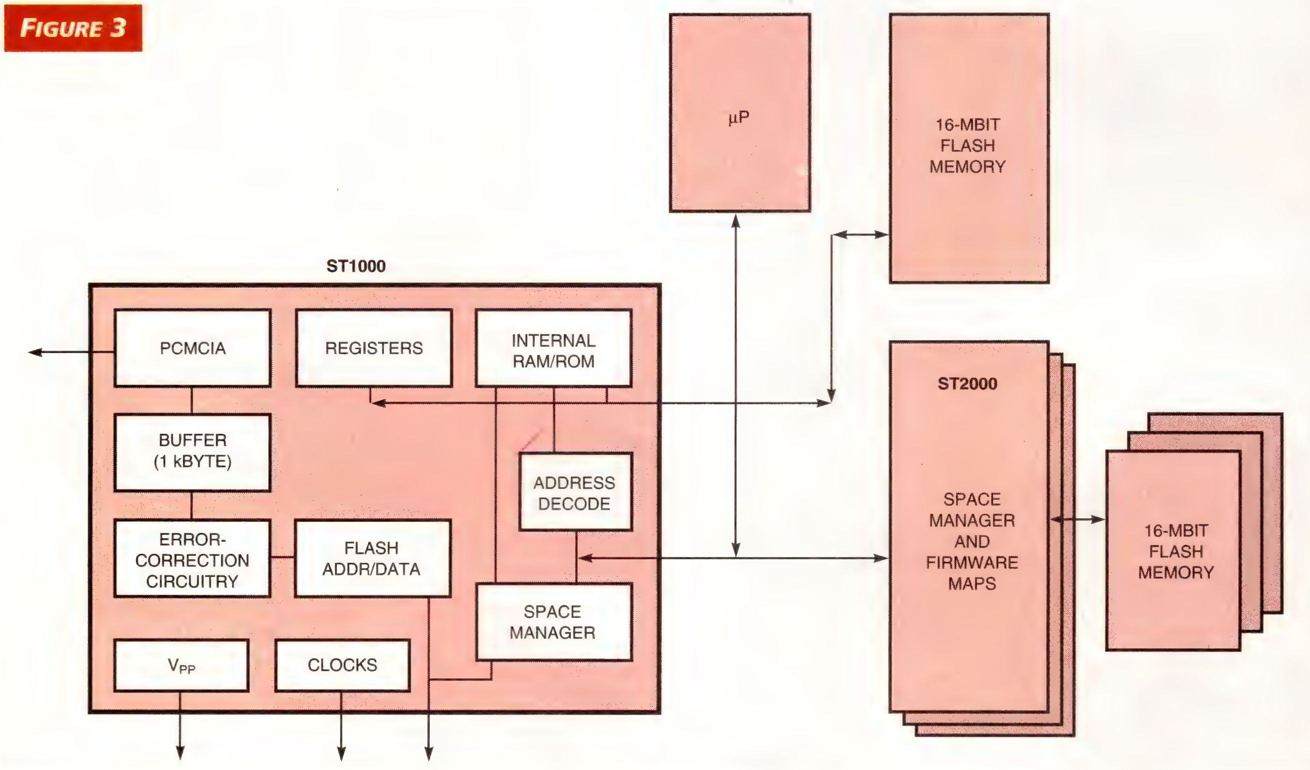
You may think that the only suitable flash devices for SSDs are those with smaller erase blocks that most closely match a disk drive's 512-byte sectors. It's true. Smaller erase blocks simplify flash-management issues. And, because the smaller blocks have faster erase times, these devices minimize the impact of having to erase before writing. On the other hand, designers have successfully built SSDs using large block flash; the trick lies in the software algorithms that manage the flash writes and erases. In the M-Systems driver, to simplify media management, designers actually grouped smaller erase blocks into larger virtual blocks.

Flash replaces DRAM

DRAM replacement and XIP represent potentially large opportunities for high-density flash. However, adapting flash to this type of application requires some fundamental software changes. Primarily, software developers separate code and data. Then, the rarely changing code is stored in (and is accessed from) flash while the system's DRAM handles the flexible data. Thus, the code is instantly available at system power-up. In battery-powered equipment, flash also enables power savings during a system suspend as a result of reducing system DRAM.

Technically, the best type of flash for this application provides fast random access. NOR flash is the only flash that currently meets this requirement. How-

FIGURE 3



Cirrus Logic's ST1000 and ST2000 provide a foundation for designing a flash drive directly on a system's motherboard or in a PCMCIA-ATA form factor.

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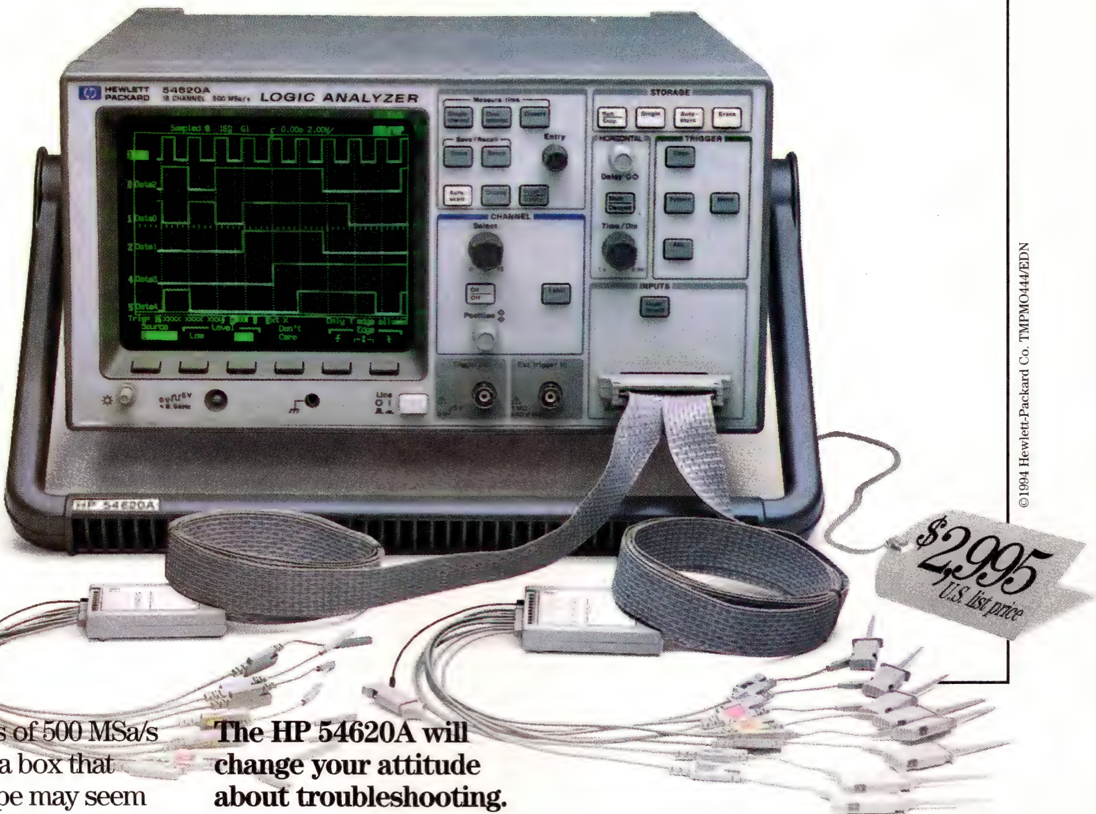

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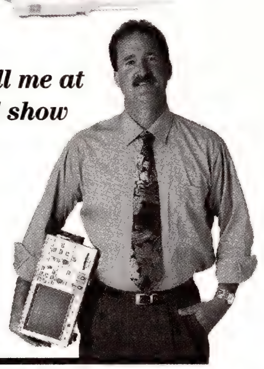

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ever, Samsung is evaluating an XIP NAND-cell architecture. Intel's 28F016XD helps system designers reduce, if not eliminate, DRAM in their systems. The 28F016XD has a multiplexed address interface with RAS# and CAS# control inputs. Designers can use the 28F016XD with a system's existing DRAM controller. Companies such as Smart Modular (San Jose, CA, (510) 623-1231) sell DRAM-compatible SIMMs based on the 28F016XD.

To allow easy code updates, designers originally used flash to replace EPROMs. Today, lower density (1- to 4-Mbit) flash devices satisfy EPROM-replacement applications; however, code-intensive systems that utilize 16-Mbit flash exist. NOR flash has been most popular as an EPROM substitute. Using NAND devices generally requires the system to have a shadow RAM to which the code copies during system initialization. Some designers perform shadowing regardless of the type of flash used if the access times are not fast enough.

Developing standards

System designers must wait patiently for standardization of flash-memory devices. Aside from architectural differences, issues such as pinouts, single- and dual-voltage supplies, write and erase algorithms, and second sourcing continue to generate confusion and concern for system designers.

The JEDEC standard has defined two fundamental flash pinouts to accommodate single- and dual-voltage supplies. The majority of flash devices has required 3.3 or 5V for V_{CC} and 12V for V_{PP} (programming voltage). In the NOR-flash camp, AMD leads the market with 5V-only devices based on negative gate erase. With negative gate erase, the device's circuitry applies 5V to the source and drives the gate negative internally. The 5V-only NAND devices have small integrated charge pumps that provide a positive voltage on the gate.

Intel has a different approach from AMD for designing its 5V-only devices. Using what the company calls Smart-Voltage technology, the devices dynamically adapt to 5 or 12V for write and erase operations, and 3.3 or 5V for reads. Special input-voltage-sensing circuitry for both V_{CC} and V_{PP} detects the system supply and internally switches the device's voltage source. Although you can tie the devices' V_{CC} and V_{PP} pins together, you can obtain higher write and erase performance (roughly twice as high) by providing V_{PP} from an external source with greater current-driving capability than the internal charge pump. SmartVoltage devices are JEDEC-compatible when used in dual-voltage mode; however, JEDEC doesn't really define a 5V-only pinout where V_{CC} and V_{PP} tie together. Nevertheless, this flexibility offers system designers a choice.

For the first five years flash was commercially available, flash manufacturers changed features so rapidly that it was difficult to establish second sources. Today, second sources are second nature. Toshiba and Samsung have a technical alliance for NAND flash development that will expire with the 64-Mbit generation. National Semiconductor committed to manufacturing Toshiba-compatible devices, but the company also has plans to produce nonstandard parts that better target specific applications such as digital cameras, for example. SGS-Thomson currently supplies a 16-Mbit device that is pinout- and software-compatible with Intel's 8-Mbit model (except for an additional address bit). SGS-Thomson will also manufacture devices that are compatible with AMD's 5V-only devices. Micron plans to produce Intel-compatible devices.

Following in the footsteps of DRAMs, flash memory is creating a market environment that draws big companies, making for a highly competitive climate. Prices continue to drop, and flash has already crossed DRAM pricing. In-Stat predicts that flash will cost less than $5 per megabyte by 1998 and that high-density flash will find its way into new applications. Initially, system designers must understand the range of flash technologies available to make the most intelligent design choices; but, ultimately, it's cost that becomes the deciding factor. EDN

LOOKING AHEAD

Flash manufacturers are actively working to drive down flash prices. Cost is a big issue for users of solid-state drives, audio storage, and digital photography. The most obvious way to reduce cost is by shrinking design rules. In the next few years, watch for process reductions down to 0.25 μm. Flash manufacturers will also move toward ensuring larger wafers, higher yields, and reduced testing time.

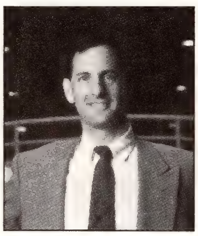
The biggest leap in density will come from an architectural improvement, named multilevel cell, that allows storage of more than 1 bit of data per cell. Multilevel cell is based on the ability to vary the voltage threshold level on a cell. Instead of a cell's being fully on (logic 0) or off (logic 1), a cell can be programmed to various degrees of "on-ness." The trick for accomplishing this lies both in controlling the programming level and precisely detecting the programmed level during reads. Such devices should begin to hit the market by the end of the year.

Reference

1. Dipert, Brian, and Markus Levy, *Designing with Flash Memory*, Annabooks, San Diego, CA, 1993.

Acknowledgment

Thanks to Jim McGregor, nonvolatile semiconductor analyst at In-Stat, for sharing his research report and market predictions for flash-memory devices.



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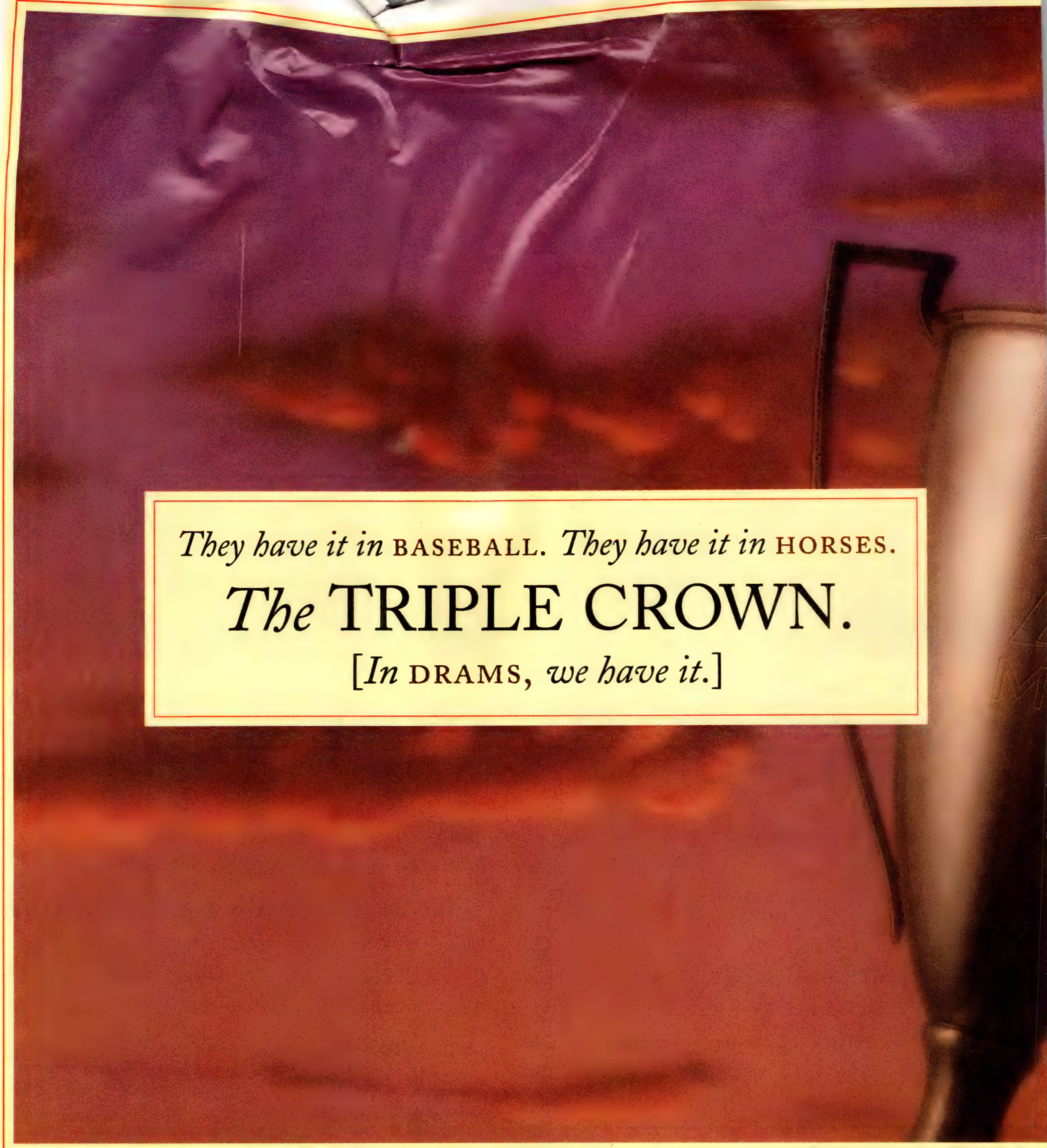

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What system designers need to know about deep-submicron ASICs

ISADORE KATZ, META-SOFTWARE INC

Strange things are happening inside ASICs as device geometries slip below 0.5 μm. Interconnect delays become much larger than gate delays, and transistors work—but not the same way they did before. Many assumptions built into ASIC design tools are no longer valid for deep-submicron IC designs. If you want to realize all of the performance of today's best IC fabrication processes, you must understand the new design requirements of the deep-submicron world.

Exploiting the full speed and complexity of deep-submicron ASICs requires knowledge of how IC physics is changing, what the resulting implications are for ASIC design tools, and how to select design tools that let you create functional deep-submicron ASICs.

The steps for getting any semiconductor product to market are the same: Develop a Spice model library for the basic devices, develop a cell library, design a chip, and insert the chip into a system. Depending on your responsibilities as a system designer, you may need to perform one or more of the last three steps. Usually, the ASIC vendor develops the Spice model libraries that describe the fundamental capabilities of the fabrication process. From these fundamentals, either you or the ASIC vendor develops the logic cells that you use to develop the various logic functions of your ASIC. Assuming everything goes well, the completed ASIC performs the desired function when you drop it into your system.

The changed physics of deep-submicron silicon structures is creating a significant discontinuity in ASIC performance as device geometries drop below 0.5 μm. **Fig 1** illustrates a typical structured-custom IC, comprising several different blocks. You may encounter a number of performance problems with these blocks. High-performance data paths require high-speed data buses and often employ timing-sensitive dynamic logic for optimum speed. RAMs contain large numbers of transistors, so they generally require the smallest transistors that the process can fabricate. Random logic blocks require complex cell libraries and often contain intricate wire routing with complex delays. Analog blocks and PLLs rely on predictable analog transistor behavior.

In each of these examples, problems arise when the ASIC design tool incorrectly models real transistor performance. As device geometries shrink below 0.5 μm, accurate modeling of transistor switching, power consumption, and the relationship between a gate and the associated interconnect becomes complex. The modeling problems stem from a breakdown in the overly simplistic models that describe the analog operation of the deep-submicron silicon structures. Some ASIC vendors have attempted to create deep-submicron Spice models by scaling existing submicron models. Models that vendors have scaled from submicron to deep-submicron IC process technology don't accurately reflect real silicon performance.

ASIC and design-tool vendors have resorted to putting an increasing amount of "fudge" in their deep-submicron specification sheets and timing tools to account for the increasing inaccuracy of the fundamental device models. Designers have actually seen delay errors of 70% between simulations and actual deep-submicron silicon performance. You can design deep-submicron ASICs this way, but you cannot achieve either the full speed that is possible from deep-submicron fabrication processes or the kind of gate densities you'd expect. You often end up in serious finger-pointing arguments with your ASIC and design-tool vendors when ASICs fail to perform at expected speeds. However, you do not have to settle for reduced performance or inefficient silicon usage. Proper modeling of the deep-submicron devices allows you to take full advantage of the silicon's underlying performance.

Deep-submicron physics mostly affects the Spice-level models. Transistor physics no longer maps neatly into the tra-

DEEP-SUBMICRON ASICS

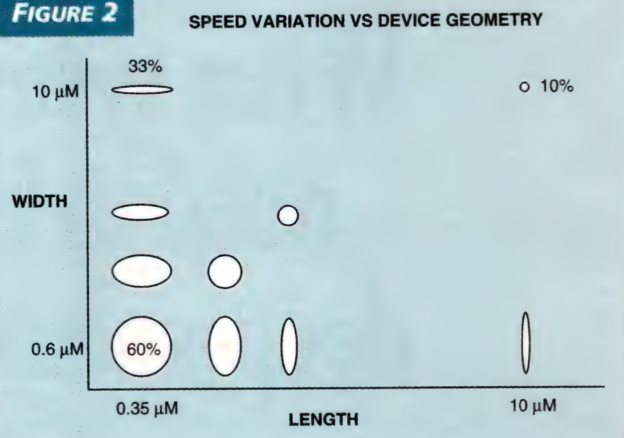
ditional Spice transistor equations for several reasons. First, the devices are finally starting to operate near their physical limits. Consider a deep-submicron FET built with an oxide thickness of 60Å. With 3V applied between the gate and the source or drain, the oxide experiences an electric field of 5 MV/cm, which is very close to the oxide's breakdown voltage. At these field strengths, second-order effects, such as impact ionization, drain-induced barrier lowering, and channel-length modulation, play an increasingly important role. Previously, Spice modeling for ASIC transistors ignored these second-order effects because they weren't needed for accurate modeling. Spice modeling for deep-submicron transistors must take these effects into account.

The second reason that Spice models must change is because the performance variance for transistors fabricated with different-sized geometries is quite large (**Fig 2**). With 0.35-μm geometries, transistor drain-to-source currents (I_{DS}) can vary ±30% from device to device on the same chip. You can see considerable lot-to-lot variation. So, I_{DS} predictability is decreasing as device geometries decrease. I_{DS} affects switching time and power dissipation.

Third, wire geometries aren't scaling with transistor geometries; the transistors are shrinking a lot faster than the wires. Consequently, the wires' resistance and capacitance are not scaling with transistor switching speeds. In fact, average wire lengths on ASICs are increasing as ASICs get larger and more complex so that wire (or interconnect) delays now dominate over gate delays. ASIC delay calculators do not properly account for wire delays. Some vendors have made linear tweaks to their submicron ASIC design tools, expecting that linear scaling can account properly for the delays at the deep-submicron level. Linear scaling can't properly model deep-submicron wire delays.

Because of these fundamental changes in device physics for deep-submicron ASICs, the HDL-to-silicon design flow of submicron ASIC design tools cracks. These existing design tools assume that wires on the ASIC behave the same whether they are short or long and logic devices can be treated as black boxes with unvarying performance.

FIGURE 2



The performance variance for transistors fabricated with different-sized geometries is quite large and can be as much as 60% (±30%) for deep-submicron processes.

The deep-submicron reality is quite different. Extremely small transistors exhibit irregular behavior. They have input-slope, load, and temperature sensitivities that design tools have never before needed to model. Further, the smaller operating voltages of deep-submicron ASICs mean that transistors must operate with a smaller transition region. The effects of a smaller transition region are evident in sensitivities to output loading and the slope of the input signal. These factors determine transistor switching speed, power consumption, and temperature. Deep-submicron transistors exhibit more sensitivity to temperature than larger devices; switching time can vary as much as ±15% due to thermal effects. In addition, although the output load of the interconnect wire in deep-submicron ASICs still looks linear because the wire has an RC impedance, the effects of the load are nonlinear because the output load affects the transistor's slew-rate sensitivity.

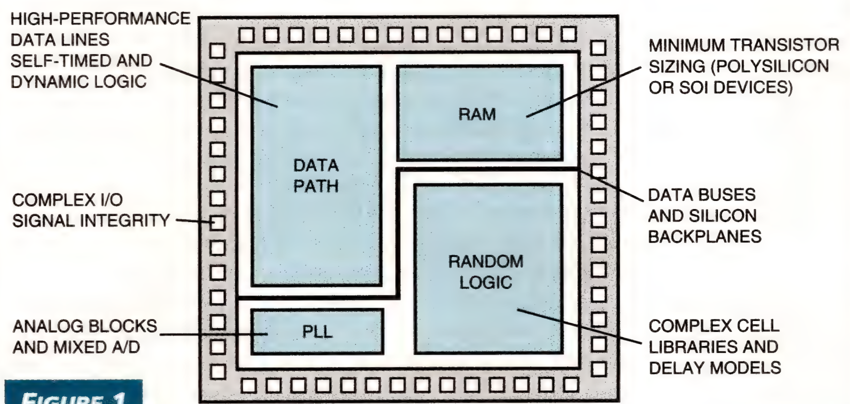


FIGURE 1

Structured custom ICs comprise several blocks—each with potential problems with deep-submicron processes. High-performance data paths require high-speed data buses and often employ timing-sensitive dynamic logic. RAMs generally require the smallest transistors that the process can fabricate. Random logic blocks require complex cell libraries and intricate wire routing with complex delays. Analog blocks and PLLs rely on predictable analog transistor behavior.

Get all the performance you buy

As the system designer, you probably have not had to deal with transistor-level effects above the submicron domain. You designed the ASIC's logic and handed the netlist to the ASIC vendor for placement and routing. Because the cell libraries were based on approximations that did a fairly good job of modeling transistor behavior, you could get by without knowing the analog nature of the fundamental devices.

DEEP-SUBMICRON ASICS

However, if you want to get your money's worth from deep-submicron fabrication processes, you must at least ask the right questions of the deep-submicron ASIC vendor to ensure that the design-tool models accurately reflect the underlying physics of the silicon.

Here are the questions to ask the deep-submicron ASIC vendor:

- Are you giving me accurate models? How do you ensure that your Spice models work over your process range? How can you provide the model parameters for your process? What performance do you guarantee?

Here are the items you need from your deep-submicron ASIC tool vendor:

- A feedback loop from the physical-design stage that provides more than just loads. More complex device-modeling libraries. A wire-model library.

There are currently three competing approaches to building a deep-submicron wire-model library: look-up tables, piecewise-linear approximations, and polynomial equations. All three approaches work, but, unfortunately, not all ASIC or design tool vendors support all types of models. You could find yourself in a spotty mix-and-match situation. Ineffective or incomplete empirical modeling of interconnect delays further complicates the situation. Most ASIC-process test chips use simple ring oscillators with first- or second-layer metal routing. Few contain the complex wire routings needed to measure actual deep-submicron wire delays. In reality, the ASIC industry must still resolve these wire-modeling and behavior-extraction problems for deep-submicron products.

Ultimately, deep-submicron ASICs put the system designer at a crossroads. If you're not exploiting the full capabilities of the deep-submicron process, you can probably continue to design as you have in the past. However, if you want to realize the full potential of deep-submicron technology and get the performance and complexity you pay for when you buy deep-submicron ASICs, then you'd better examine your ASIC and ASIC tool vendors more closely than you ever have before. EDN

Author's biography

Isadore Katz is the vice president of marketing at Meta-Software. He has served as the vice president of marketing at Cadence's IC Design Division and has held senior positions at Daisy Systems and EDA Systems. He has been a senior industry analyst at Dataquest.

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Switching regulator controls CCFT

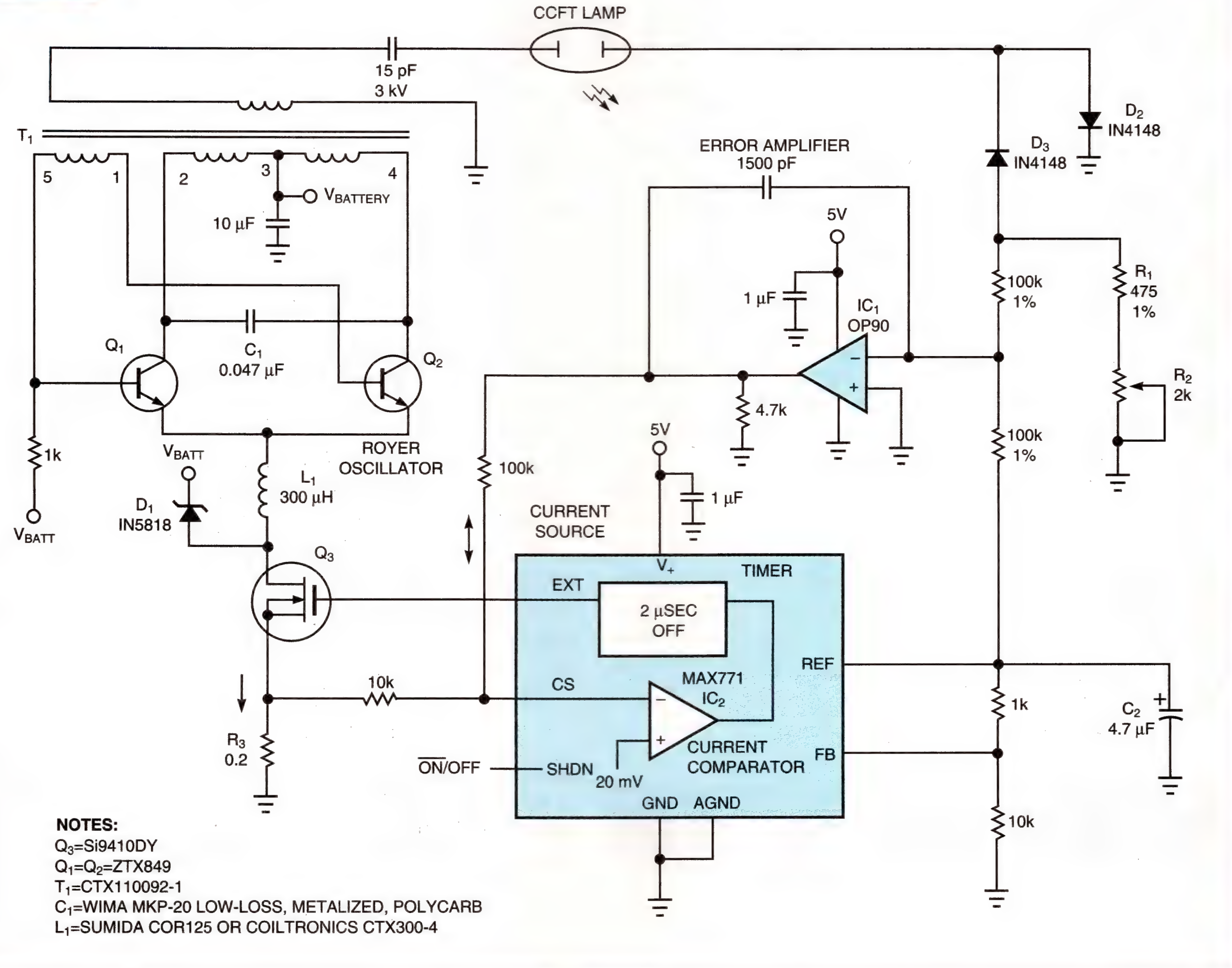
DOUG VARGHA, MAXIM INTEGRATED PRODUCTS, SUNNYVALE, CA

You can control the current in a cold-cathode fluorescent tube (CCFT) and, hence, its brightness with a switching-regulator IC. Often used as a backlight, a CCFT requires an adjustable, high-voltage, ac-power source. EMI and tube-lifetime considerations dictate a sinusoidal waveform. A resonant circuit is best for generating sinusoids.

One of the simplest oscillators is the Royer type—a self-oscillating, current-fed, parallel-resonant power oscillator (**Fig 1**). The Royer oscillator comprises T_1 and its secondary load, C_1, Q_1, and Q_2. The effective inductance and capacitance of T_1's primary winding determine self-oscillating frequency. An auxiliary winding (T_1's pins 5 and 1) drives Q_1 and Q_2. The oscillator does not require capacitors at the emitters of Q_1 and Q_2 to work because L_1 holds the current constant at Q_1's and Q_2's emitters. The circuit has a bypass capacitor at the input to the resonant circuit (T_1's center tap).

A current source, comprising L_1, D_1, and Q_3, feeds the oscillator. IC_1 and IC_2 control this current source. D_3 and D_2 rectify the tube's current. Half of that current develops a negative voltage across R_1 and R_2, producing a current that bal-

FIGURE 1



Employing IC_1 as an error amplifier and using just the current-mode control of regulator IC_2, this circuit adjusts a CCFT's brightness by varying the output of a Royer power oscillator.

ances current from the 1.5V reference (pin 5, IC_2). An increase in the error amplifier's output increases the negative voltage by increasing the tube's current and vice versa. Brightness varies from maximum to minimum as you adjust R_2 from 0 to 2 kΩ.

IC_2 is a step-up switching regulator that normally employs both voltage and current feedback to control the MOSFET switch, Q_3. Holding IC_2's FP pin (pin 3) below its REF (pin 5) confines this IC to the current-feedback mode.

IC_2's internal current-feedback controls comprise a comparator, which turns switch Q_3 off, and a timer, which turns it on. Turning switch Q_3 on causes its current to ramp up, which, in turn, causes the voltage at IC_2's CS pin to ramp up. When the CS voltage reaches 210 mV, IC_2's comparator turns switch Q_3 off. Then, the current in Q_3 quickly ramps down, and the timer holds switch Q_3 off for 2 μsec before turning Q_3 on again.

By sinking or sourcing current, the error amplifier, IC_1, affects the maximum (peak) current through current-sense resistor R_3.

At power-up, the circuit must start gradually to avoid secondary-voltage overshoots that might damage the transformer. Capacitor C_2 provides a soft start by causing IC_2's internal, current-limited V_{REF} to slowly approach its nominal 1.5V level. Because the current comparator's voltage threshold (derived from the reference) rises slowly as well (toward 210 mV), the peak inductor current rises slowly, thereby eliminating overshoot at the transformer's secondary.

The minimum gate voltage of Q_3 sets the lower limit for the circuit's input voltage. The maximum voltage depends on the regulator and op amp you use (12V for components shown). Input V_{BATT} must be greater than 6.5V and one diode drop less than Q_3's absolute maximum drain-to-source voltage (30V). Raising T_1's turns ratio lowers the minimum voltage needed for V_{BATT}. (DI #1657) EDN

To Vote For This Design, Circle No. 454

Cubic interpolation hikes table's accuracy

Brad Eckert, Industrial Commercial Electronics, Buffalo, NY

You can obtain very accurate approximations of a function from only a few data points contained in a look-up table, trading storage space for calculation time. For example, you can derive $\log_2(1...2)$ and $\sin(1...\pi/2)$ functions to 16-bit accuracy from only 18 data points.

Cubic interpolation takes into account the curvature of a function by using the beginning and ending slopes of a curve segment to approximate the missing curve with a cubic polynomial. Taking four data points, P_0, P_1, P_2, and P_3, from a table, cubic interpolation approximates the curve connecting P_1 and P_2 and returns the value corresponding to any point along that curve between P_1 and P_2.

The theory of cubic interpolation begins with the cubic function

$$f(x)=w_0+w_1\times x+w_2\times x^2+w_3\times x^3$$

that defines a curve between points P_1 and P_2. To simplify the math, assume that variable x ranges from only 0 to 1.

You must set the coefficients, w_0, w_1, w_2, and w_3, so that the cubic polynomial satisfies these four initial conditions:

- **(1)** $f(0)=y_1$ value at P_1
- **(2)** $f(1)=y_2$ value at P_2
- **(3)** $f'(0)=(y_2-y_0)/2$ slope at P_1
- **(4)** $f'(1)=(y_3-y_1)/2$ slope at P_2

Differentiating f(x) twice yields two more equations:

- **(5)** $f'(x)=w_1+2w_2\times x+3w_3\times x^2$
- **(6)** $f''(x)=2w_2+6w_3\times x$.

You can immediately derive w_0 and w_1 from initial conditions **1** and **3**. Using initial conditions **2** and **4**, you can solve **Eqs 5** and **6** for w_2 and w_3.

The resulting coefficients are

- $w_0=y_1$ initial value
- $w_1=(y_2-y_0)/2$ initial slope
- $w_2=(-y_3+4y_2-5y_1+2y_0)/2$ initial curvature
- $w_3=(y_3-3y_2+3y_1-y_0)/2$ rate of change of curvature

Table 1 contains example interpolations for a sloping line, a parabola, and an arbitrary curve.

Table 1—Sample cubic-interpolation calculations

Curve	Data set f(x)=	w_1	w_2	w_3	f(0.5)
Sloping line	6,7,8,9	1	0	0	7.5
Parabola	5,7,7,5	1	−1	0	7.25
Arbitrary curve	1,2,3,1	1	1.5	−1.5	2.6875

To use cubic interpolation with fast-integer math on unsigned numbers, first scale the function by defining $n=2^{cell\_size}\times x$. The *cell_size* depends on your processor and is usually 8, 16, or 32. Plugging in n, the scaled function becomes

$$f(n)=w_0+w_1\times n/2^{cell\_size}$$
$$+w_2\times n/2^{cell\_size}\times n/2^{cell\_size}$$
$$+w_3\times n/2^{cell\_size}\times n/2^{cell\_size}\times n/2^{cell\_size}$$

With the function properly scaled, you can drop the lower half of products after multiplying. Be sure to wait until you have completed a computation before throwing away the lower half of a double-precision integer calculation because the fractions could easily sum to more than 1 LSB.

You do not need a "powers" function if you evaluate the function as

$$f(x)=((W_3\times x+W_2)\times x+W_1)\times x+W_0.$$

(DI #1655) EDN

To Vote For This Design, Circle No. 455

Commutating amp performs log function

MOSHE GERSTENHABER AND STEFANO D'AQUINO, ANALOG DEVICES, WILMINGTON, MA

Customarily, logarithmic amplifiers exploit the V/I characteristic of a pn junction or approximate a log function in a piecewise-linear fashion. Both approaches suffer from inherent limitations. A pn junction's V/I characteristic has large temperature coefficients requiring ad hoc compensation circuitry. Piecewise-linear approximations exhibit discontinuities in their first derivatives.

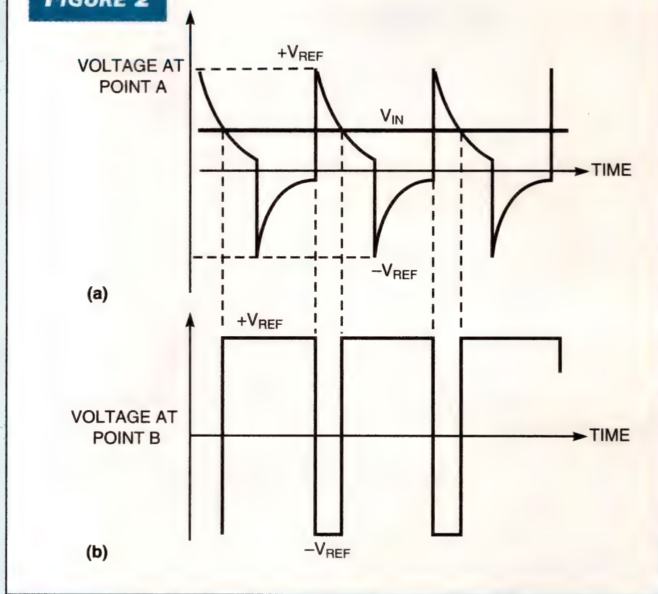
The circuit in **Fig 1** is a true log amp having no junction-generated thermal terms for which to compensate and no discontinuities in its first derivative over its full useful range.

Commutating amp IC_1, voltage reference IC_5, capacitor C_1, and resistors R_1 through R_3 make an oscillator having a frequency (f) of

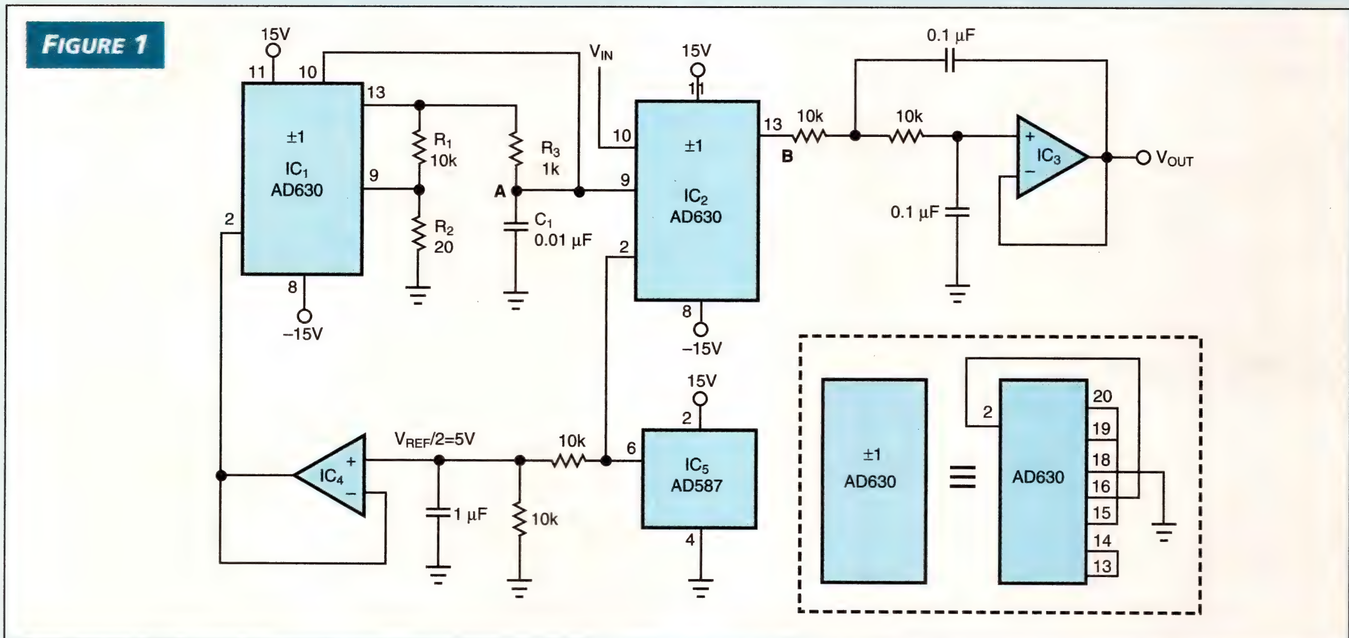
$$f=\left(2R_3C_1\ln\frac{2R_1}{R_2}\right)^{-1}.$$

$$V_{OUT}=\frac{V_{REF}}{\ln\frac{2R_1}{R_2}}\cdot\ln\frac{V_{IN}}{\frac{R_2}{2R_1}V_{REF}},$$

$$V_{OUT}=\frac{V_{REF}}{3}\cdot\text{Log}\frac{V_{IN}}{10\ \text{mV}}. \qquad (1)$$



IC_1's output in (a) is logarithmic. In (b), comparing the input voltage, V_{IN}, to IC_1's output produces a variable-duty-cycle square wave.



Commutating amp IC_1 is part of an oscillator whose output-voltage waveform is logarithmic. IC_2 compares this waveform to the input voltage, V_{IN}, producing a square wave whose duty cycle is proportional to the log of V_{IN}.

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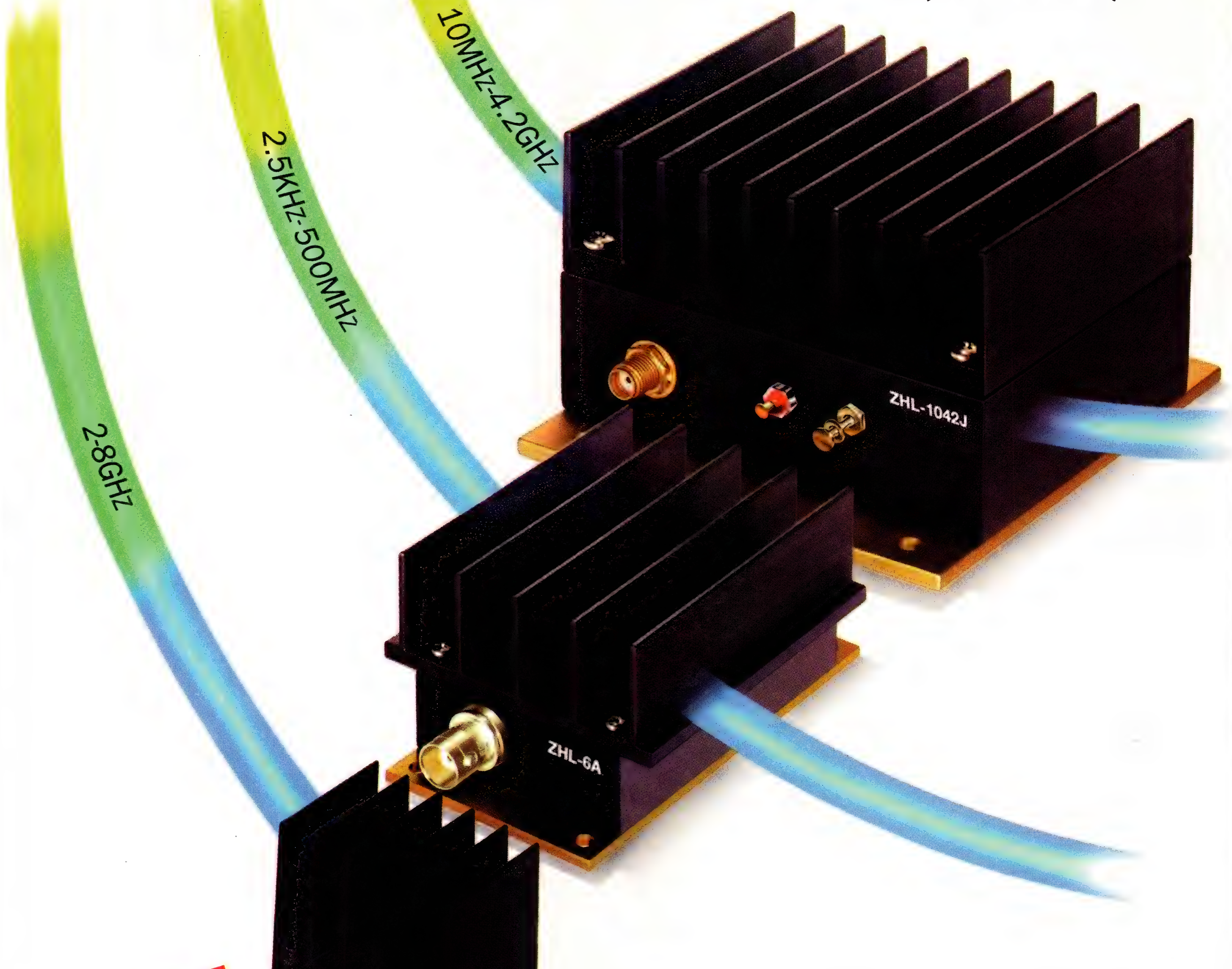

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CIRCLE NO. 121

The voltage at point A in the circuit (also see **Fig 2a**) exhibits a true exponential form. The circuit then compares this voltage with the input voltage, V_{IN}, yielding a square wave whose duty cycle increases with V_{IN} (peak values are $\pm V_{REF}$ (see **Fig 2b**)). Lowpass filtering then produces the final output

$$V_{OUT} = \frac{V_{REF}}{3} \bullet \mathrm{Log}\frac{V_{IN}}{10\ \mathrm{mV}} \quad \text{for} \quad V_{IN} > \frac{V_{REF}}{2} \bullet \frac{R_2}{R_1}, \qquad \textbf{(2)}$$

which after numerical substitution yields

$$V_{OUT} = -\frac{V_{REF}}{3} \bullet \mathrm{Log}\left(-\frac{V_{IN}}{10\ \mathrm{mV}}\right) \quad \text{for} \quad V_{IN} < -\frac{V_{REF}}{2} \bullet \frac{V_2}{R_1}. \qquad \textbf{(3)}$$

The constants in **Eq 1** depend only on the values of R_1 and R_2. Because of symmetry, the circuit produces an output for both positive and negative values of V_{IN} such that V_{OUT} always obeys **Eqs 2**, **3**, and **4**.

$$V_{OUT} = 0 \quad \text{for} \quad -\frac{V_{REF}}{2} \bullet \frac{R_2}{R_1} < V_{IN} < \frac{V_{REF}}{2} \bullet \frac{R_2}{R_1}. \qquad \textbf{(4)}$$

(DI #1658) EDN

To Vote For This Design, Circle No. 456

Graphics controller handles interleaved memory

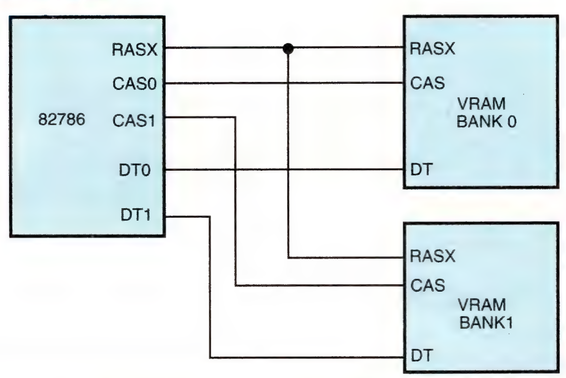
YS TAM, CANADIAN MARCONI CO, KANATA, ON, CANADA

The Intel 82786 graphics controller does not generate a proper data-transfer cycle if your video RAM (VRAM) is organized into two interleaved banks (**Fig 1**). The circuit in **Fig 2** overcomes this device's deficiency.

A video controller's data-transfer cycle must load the VRAM's shift register from the selected address during the video-blanking period. During normal read or write cycles, IC_3's _Q output in **Fig 2**, is at a logic high. This state allows _CAS0 and _CAS1 to pass through without any changes. During data-transfer cycles, IC_3's pin 6 goes low after the falling edge of _CAS0. This change extends the duration of _CAS0 and _CAS1 until the end of the cycle. (DI #1659) EDN

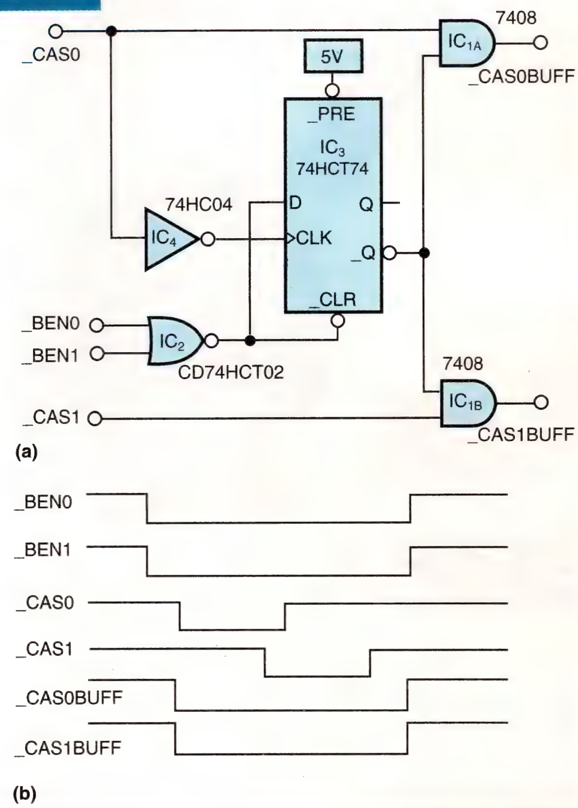
To Vote For This Design, Circle No. 457

FIGURE 1



An Intel 82786 cannot handle interleaved video RAM (VRAM).

FIGURE 2



This circuit (a) extends the durations of _CAS0 and _CAS1 signals during data-transfer cycles (b), allowing the graphics controller to access interleaved video memory.

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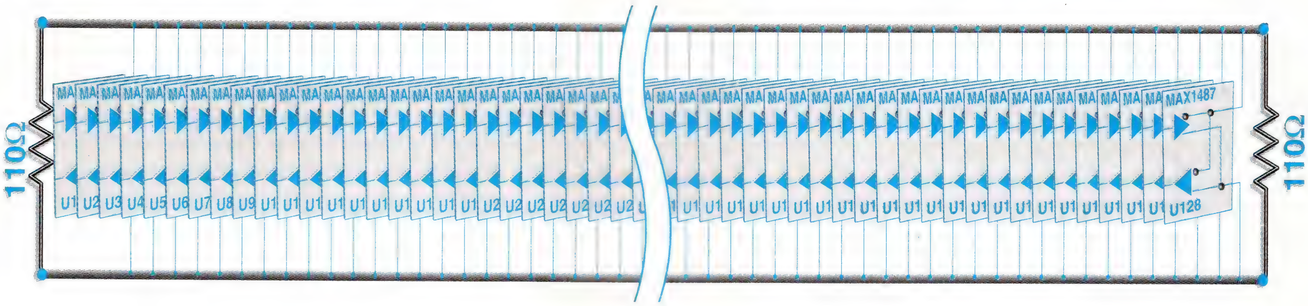

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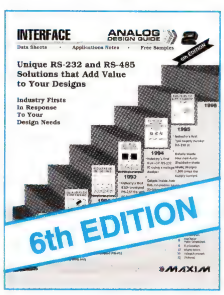

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CIRCLE NO. 110

LIER circuit helps power-supply efficiency

BRIAN POINDEXTER, ALLIED SIGNAL AVIONICS INC, OLATHE, KS

In high-frequency, high-power, low-input-voltage, flyback-converter power supplies, parasitic effects become overwhelmingly problematic. The flyback inductor's required primary inductance, for example, can become so low that its accompanying leakage inductance becomes a significant fraction of the total inductance. The energy stored in the primary leakage inductance lowers the circuit's efficiency and increases the power-rating requirements for the primary-winding switching device.

The leakage-inductance, energy-recovery (LIER) circuit in **Fig 1** recovers energy stored in the primary leakage inductance and delivers the recovered energy to one of the power supply's outputs. Ideally, the energy transfer should be completely reactive. In this circuit, recovered energy transforms from the inductor's leakage-inductance current to C_3's voltage, from C_3's voltage to L_1's current, and from L_1' current to C_O's voltage.

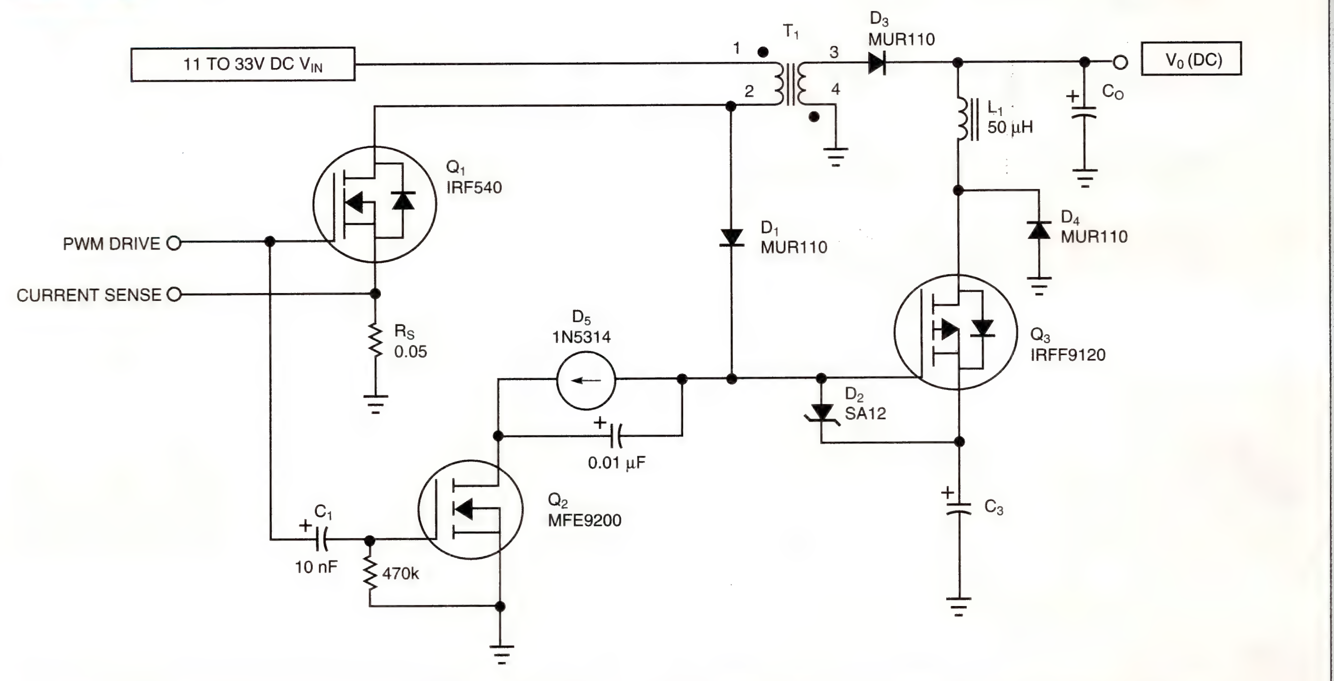
T_1, Q_1, R_S, D_3, and C_O compose the familiar discontinuous-mode flyback converter (**Fig 1** shows only one secondary winding of T_1 for clarity). Flyback action occurs when Q_1 turns off at the end of a primary-charging period. At this point, Q_2, an n-channel MOSFET, also turns off.

The voltage at the drain of Q_1 follows the rising edge of the leakage-inductance spike at point A. When the voltage at point A starts to exceed the voltage across C_3, D_1 (MUR110) and D_2 (zener SA12A) conduct in the forward mode, causing the energy stored in the leakage inductance to transform into voltage across C_3.

When the leakage inductance has released all of its energy, the voltage across C_3 reaches its maximum value. The energy transferred to C_3 equals the leakage inductance's energy plus the energy associated with the average current sourced by the primary flyback pulse (as the current flowing in the leakage inductance returns to zero). D_1 now becomes reversed-biased, thus maintaining C_3's voltage at a constant level until a new primary-charging period begins.

When Q_1 turns on for the next primary-charging period, Q_2 likewise turns on, causing zener current to flow in D_2. D_5, a 1N5314, functions as a 5-mA current source to keep D_2 biased on. The voltage across D_2 turns on Q_3, a p-channel power MOSFET. C_2 speeds Q_3's turn-on. C_3 then discharges through Q_3, transferring its energy to L_1 as the current in L_1 increases. During this interval, energy also flows into C_O (manifested as an average current flow into C_O).

FIGURE 1



This high-frequency, high-power, low-input-voltage, flyback-converter power supply conquers efficiency-killing parasitic effects. Energy recovered from the inductor's leakage inductance flows to C_3, from C_3 to L_1, and, last, from L_1 to C_O.

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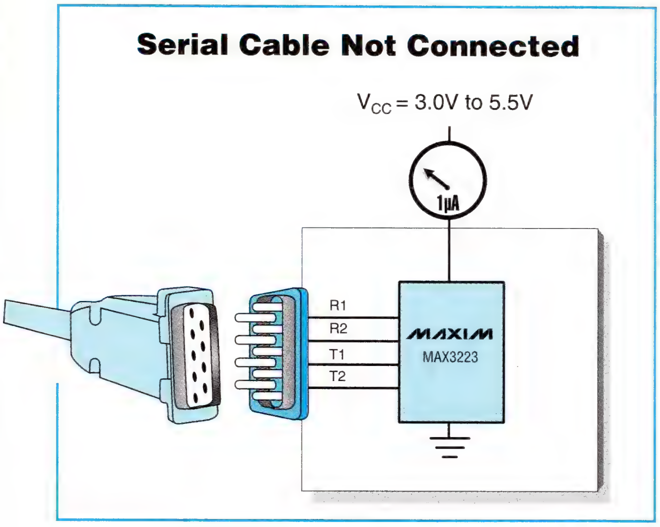

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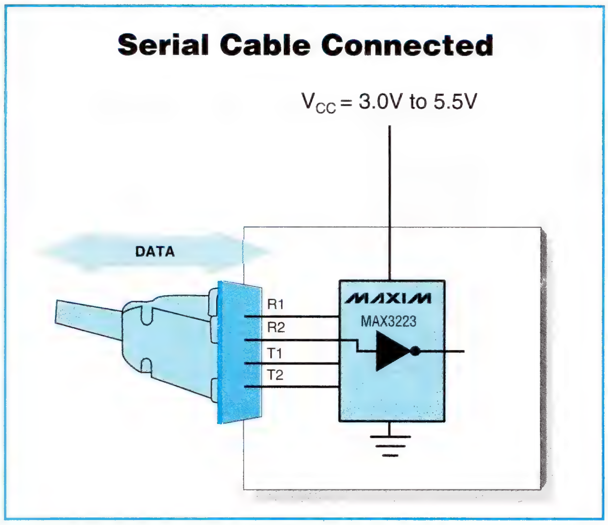

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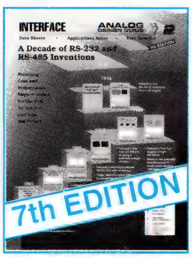

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CIRCLE NO. 112

When Q_1 turns off again, Q_2 and Q_3 likewise turn off. D_4 then allows L_1 to transfer its stored energy to C_O as L_1's current returns to zero.

When C_3 is "large," the following relation summarizes the LIER circuit's effect on overall power-supply efficiency:

η_T =total power-supply efficiency,
P_O =power delivered by the supply,
P_{IN} =power delivered by V_{IN} to the supply,
η_C =flyback transformer-core efficiency,
L_M =primary-winding mutual (total–leakage) inductance,
L_P =total primary inductance (mutual+leakage),
L_L =primary-winding leakage inductance,
LEF =LIER efficiency factor, the ratio of the peak current in D_1 to the peak current in the primary winding. An LEF of 1 results in the ideal lossless case (determined empirically, typical values range from 0.5 to 0.7),
V_{IN} =input voltage to the supply, and
V_{FB} =primary-winding flyback voltage.

$$\eta_T = \frac{P_O}{P_{IN}} = \frac{\eta_C L_M + LEF\left(\frac{V_{IN}}{V_{C3} - V_{FB}} + 1\right)L_L}{L_P + LEF\left(\frac{L_L V_{IN}}{V_{C3} - V_{FB}}\right)},$$

$$V_{C3} = \frac{V_{FB} + V_O + \sqrt{\left(V_{FB} - V_O\right)^2 + \left(LEF\right)\left(\frac{V_{IN}}{L_P}\right)^2 L_1 L_L}}{2},$$

where V_{C3}=dc voltage across C_3.

With no LIER circuit contribution (LEF=0), the total efficiency reverts back to the ratio of mutual inductance to total primary inductance (ignoring core efficiency). The compressed ZIPfile attached to **EDN BBS /DI_SIG #1660** contains a copy of this write-up and artwork cleverly drawn in IBM characters as well as a more detailed exposition. (DI #1660) EDN

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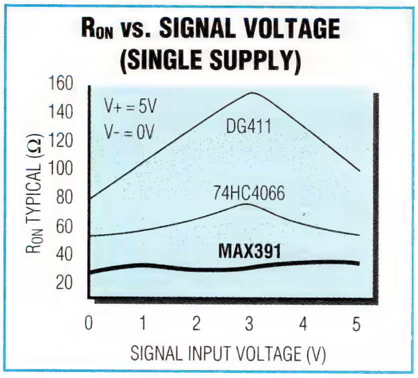

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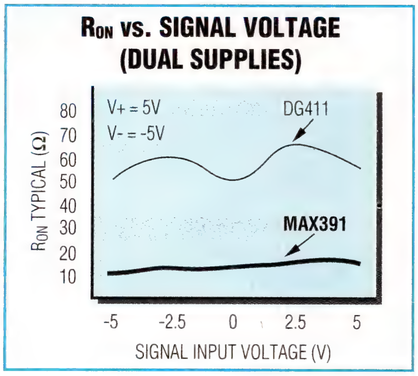

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DEVICE	FUNCTION	ON-RESISTANCE MATCH (Ω max)	ON-RESISTANCE FLATNESS (Ω max)	CHARGE INJECTION (pC max)	PIN COMPATIBLE	μMAX PACKAGE
MAX320	Dual SPST (NO)	2	6	5		✔
MAX321	Dual SPST (NC)	2	6	5		✔
MAX322	Dual SPST (NO, NC)	2	6	5		✔
MAX323	Dual SPST (NO)	2	6	5		✔
MAX324	Dual SPST (NC)	2	6	5		✔
MAX325	Dual SPST (NO, NC)	2	6	5		✔
MAX381	Dual SPST (NO)	2	6	5	DG401	
MAX383	Dual SPDT	2	6	5	DG403	
MAX385	Dual DPST (NO)	2	6	5	DG405	
MAX391	Quad SPST (NC)	2	6	5	DG411	
MAX392	Quad SPST (NO)	2	6	5	DG412	
MAX393	Quad SPST (NO, NC)	2	6	5	DG413	
MAX396*	16-Channel Mux	10	16	5	DG406	
MAX397*	Dual 8-Channel Mux	10	16	5	DG407	
MAX398	8-Channel Mux	10	16	5	DG408	
MAX399	Dual 4-Channel Mux	10	16	5	DG409	

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The winning Design Idea for the September 1, 1994, issue is entitled "Solid-state relay saves battery's life," submitted by Tom Gay of Siemens (Regensbury, Germany).

LINEAR TECHNOLOGY DESIGN NOTES

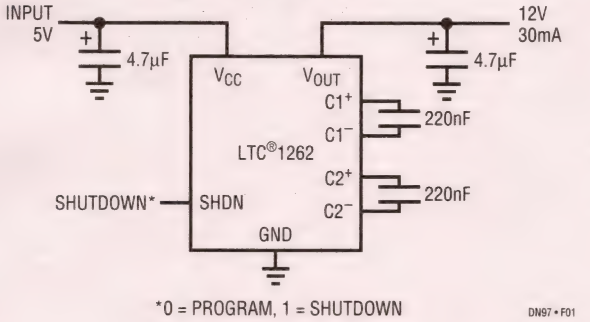
Flash Memory VPP Generator Reference Designs

Design Note 97

Mitchell Lee

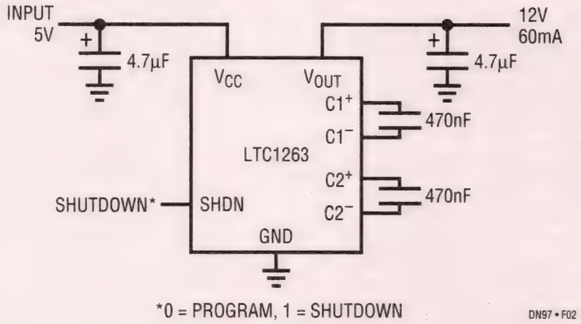
The VPP generator circuits shown here cover a range of 30mA to 240mA with 3.3V or 5V inputs as noted. Table 1 summarizes these circuits for quick reference.

30mA from 5V Input



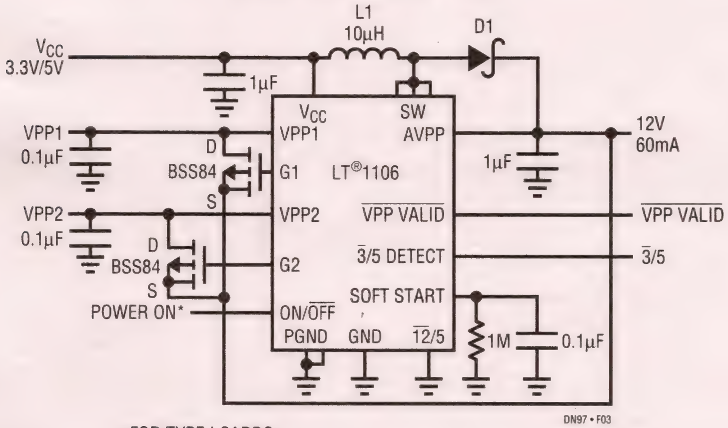
Charge pump design uses no inductors. This is a minimum component count, minimum size solution.

60mA from 5V Input



Charge pump design uses no inductors. This is a minimum component count, minimum size solution.

60mA from 3.3V/5V Input



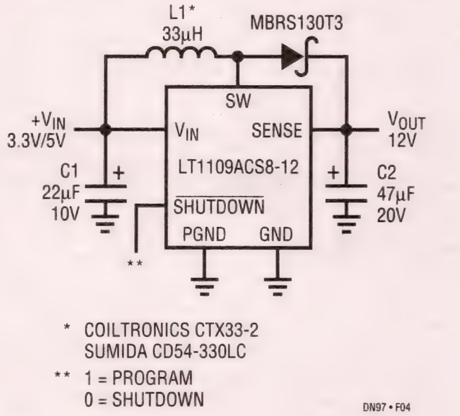
FOR TYPE I CARDS:
L1: DALE ILS-3825-01
D1: 4 BAT54Cs IN PARALLEL (PHILIPS), 1.1mm MAXIMUM HEIGHT

FOR TYPE II CARDS:
L1: MURATA ERIE LQH3C100K04M00
D1: MOTOROLA MBRS0520, 2.1mm MAXIMUM HEIGHT

*1 = PROGRAM, 0 = SHUTDOWN

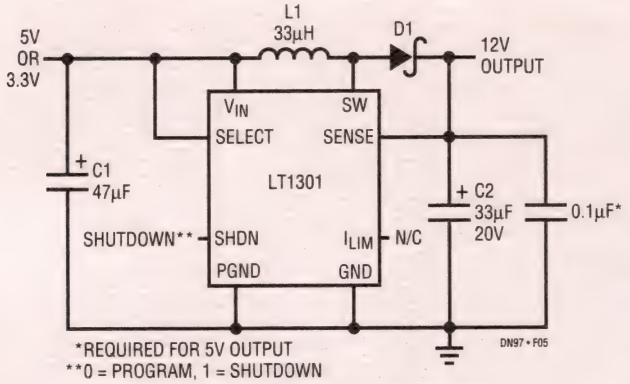
Designed for PCMCIA Type I or Type II in-card use. The LT1106 includes VPP bank switching for up to four memory chips.

60mA/120mA from 3.3V/5V Input



All surface mount, minimum component count solution.

60mA/120mA from 3.3V/5V Input

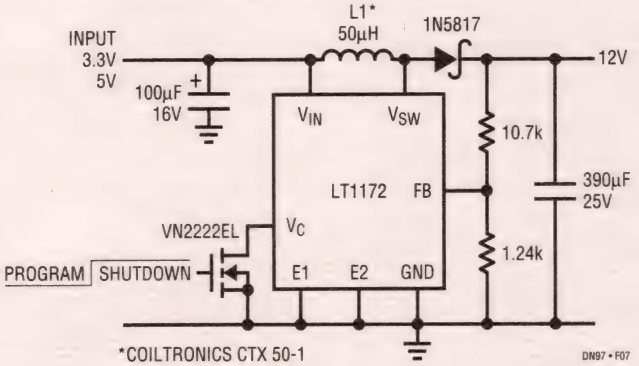


*REQUIRED FOR 5V OUTPUT
**0 = PROGRAM, 1 = SHUTDOWN

L1: COILCRAFT DO3316-333 OR SUMIDA CD73-330KC
D1: 1N5817 OR MOTOROLA MBRS130LT3
C1: AVX TPSD476M016R0100 OR SANYO OS-CON 165A47M
C2: AVX TPSD336M020R0100 OR SANYO OS-CON 205A33M

Efficiency is 84% to 88% at full load.

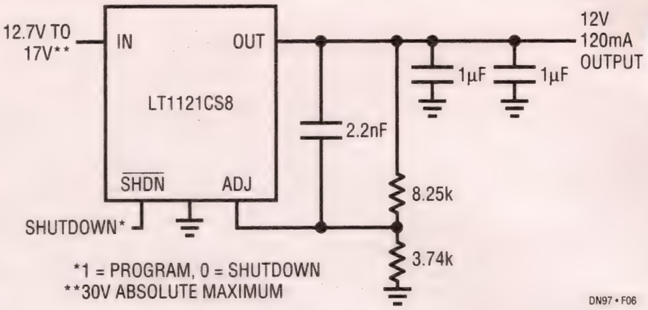
120mA/240mA from 3.3V/5V Input



*COILTRONICS CTX 50-1

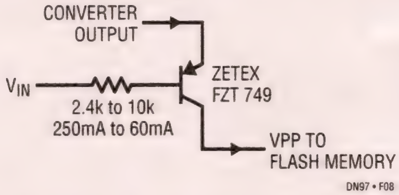
High output current converter programs up to eight memory chips simultaneously.

120mA from 12.7V to 17V Input



This circuit serves as a post regulator for flyback converters or overwindings. Output automatically falls to zero in shutdown.

Output Disconnect



This shutdown circuit allows output to drop to zero when switching converter is disabled.

Table 1. Summary of Flash Memory VPP Generator Solutions

Number of Flash Chips				
V_{IN} = 3.3V	V_{IN} = 5V	V_{IN} = 12.6V To 17V	Regulator	Advantages
—	1	—	LTC1262	No Inductors
—	2	—	LTC1263	No Inductors
2	2	—	LT1106	PCMCIA Type I In-Card Use. Includes VPP Bank Switching for 4 Memory Chips
2	4	—	LT1109A	Low Cost
2	4	—	LT1301	High Efficiency
—	—	4	LT1121	Linear Post Regulator
4	8	—	LT1172	High Current

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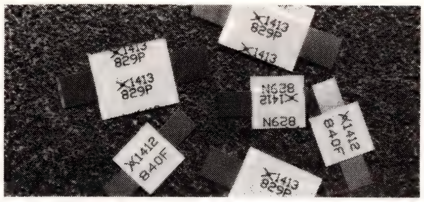
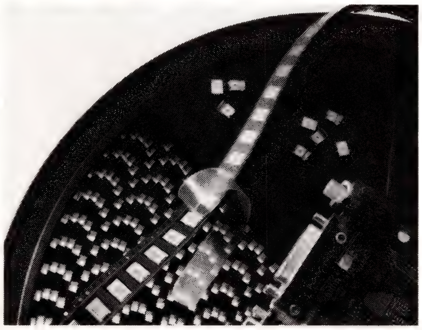
OVERCURRENT PROTECTION FOR BATTERY PACKS



Designed specifically for NiCad batteries, Raychem's new line of PolySwitch devices provides resettable discharge-overcurrent protection in a package that can be welded directly into battery packs. The new devices offer higher current ratings in a smaller size than previously available, and can be used over a wider temperature range.

CIRCLE NO. 157

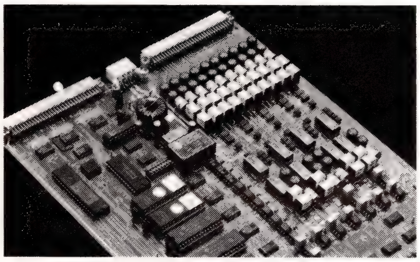
RAYCHEM'S POLYSWITCH SURFACE-MOUNT DEVICES PROTECT COMPUTERS, LANS



PolySwitch surface-mount circuit protection devices from Raychem Corporation provide reliable, resettable circuit protection for computers and local area networks. Installed on printed-circuit boards in the DC power-feed circuit, the devices protect computer and communications equipment in the event of an electrical fault or overload. Because they are resettable, PolySwitch protectors eliminate the problem of blown fuses and related equipment repairs.

CIRCLE NO. 160

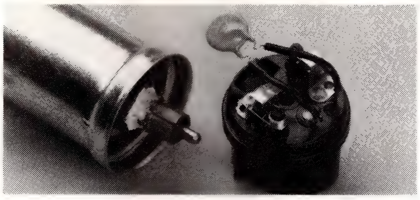
RESETTABLE TELECOMMUNICATIONS PROTECTION, UL 1459 APPLICATIONS



Raychem's PolySwitch devices provide resettable overcurrent protection in telephone interface applications. When an overcurrent hazard happens on a tip/ring interface, PolySwitch devices effectively limit current, then return the circuit to normal operation once the fault subsides. When used in appropriately designed tip/ring circuits, PolySwitch devices allow telecommunications equipment to meet UL 1459, the customer-premises telephone equipment safety standard.

CIRCLE NO. 161

POLYSWITCH RESETTABLE FUSES IDEAL FOR DC MOTORS



Solid-state PolySwitch circuit protection devices from Raychem provide resettable overcurrent and overtemperature protection for DC motors. The devices are widely used in automotive motors and actuators that control power door locks, windows and seats. Other applications include solenoid and motor protection in computer peripherals, ATM machines, and cooling fans. PolySwitch devices have no moving parts, no contacts to arc, are insensitive to vibration, and can be custom designed.

CIRCLE NO. 158

POLYSWITCH RXE FAMILY HAS WIDE RANGE OF USES

The RXE general-purpose line of PolySwitch circuit protectors from Raychem is well-suited for power supplies, alarm systems, speakers, motors, telecommunications and many other applications. The durable devices handle normal currents from .10 to 3.75 amps and are rated at 50 or 60 volts. They require no manual resetting or replacement, and won't damage circuits by continuously cycling. Some devices are available on tape-and-reel for auto insertion.

CIRCLE NO. 159

Deep-submicron ASIC design requires design planning

BOB WIEDERHOLD, HIGH LEVEL DESIGN SYSTEMS

IC designers moving to deep-submicron technologies face big challenges. Initial design projects have experienced unexpectedly long design cycles, many design iterations, problems getting chips to operate at target clock speeds, and surprises with die size late in the design cycle. The effects of deep-submicron geometries, higher clock speeds, and soaring gate counts all create design problems existing tools and methodologies do not address.

The limitations of available tools and methodologies for deep-submicron IC design are clear. Logic designers, who once needed to know little about the physical implementation of their devices to successfully complete their designs, must now have access to key physical-design information early in the design cycle. Without this information, designers cannot accurately predict timing delays, routability, and power dissipation. Further, designers have no way of knowing if their designs are meeting such basic design constraints as function, cost, power, and speed. The result is often big surprises late in the design cycle.

Avoiding these surprises involves improving the early design process. Logic designers must have insight into physical-implementation realities without performing detailed placement and routing. A relatively new tool, the "design planner," can provide this information. As most of the IC market moves to 0.5 μm and smaller feature sizes, this design planning will become a critical part of every leading-edge IC-design team's methodology (**Fig 1**).

Breakdown of old methodologies

Current methodologies rely on the assumption that, during logic design, using little more than a netlist and statistical models of interconnect characteristics, designers can accurately predict timing delays, routability, size, and power dissipation. Before the advent of deep-submicron technologies, designers did not need information about a design's actual physical implementation to make accurate predictions. As a result, logical and physical design remained separate. In most cases, designs required only one iteration between the logical- and physical-design phases.

This model does not hold true for deep-submicron designs, however. Today's design tools no longer accurately predict delay, routability, size, and power dissipation unless the designer provides information about the physical implementation. For example, designers cannot make rough estimates about interconnection, which now plays a dominant role in delay and power dissipation. The use of macro blocks, larger data buses, and synthesis tools has created severe routability problems that designers cannot predict using simple netlist analysis.

Designers that continue to use older design methodologies experience big problems with deep-submicron IC designs. They don't discover timing, routability, size, and power problems until they perform detailed placement and routing. Multiple, lengthy iterations ensue between the logic and physical designer to repair these problems. The end result is that iterations between logic and physical designers grow from one to three iterations for 0.8-μm designs to more than 10 iterations for designs with 0.6-μm and smaller features. With each full iteration requiring an average of one to six weeks, these extra design iterations add considerable time to the design cycle (**Fig 2**).

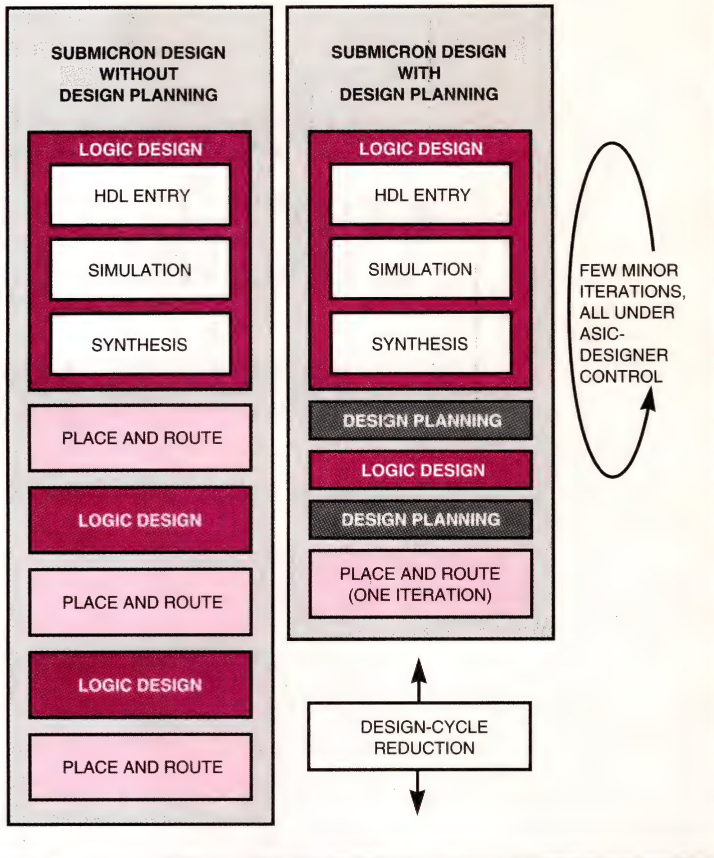
To accurately predict interconnect effects during logic design, designers must develop a design's floor plan and precisely predict the placement of cells and the routing of nets.

DEEP-SUBMICRON ASIC DESIGN

A floor plan provides a high-level abstraction of the eventual physical implementation of a design. However, you can quickly create and modify a floor plan, which you cannot do with a final placement and routing. As a result, a floor plan allows you to quickly complete multiple iterations with synthesis and timing-analysis tools and to resolve timing-, size-, and power-constraint problems. Because a floor plan provides the logic designer with key physical-design information, tools that employ floor-plan information can solve problems during logic design when they are least expensive to fix. If the final logic design accounts for the physical implementation of the design, a single placement-and-routing cycle should produce a successful design, significantly reducing design times.

You use a design-planning tool to quickly isolate and resolve problems during logical design. A floor planner, on the other hand, deals only with the physical, geometrical aspects of physical-IC design, such as block-aspect-ratio sizing and pin-location optimization. A design planner provides a range of technologies that go far beyond the traditional capabilities of a floor planner, adding technologies that accurately predict delays, routability, and power dissipation. Information about these problems allows you to make critical design changes early in the design cycle.

FIGURE 2



Current design methodologies often require 10 or more design iterations between the logic designer and physical designer. By inserting design planning into the logic-design phase, you can avoid lengthy place-and-route iterations.

You create a floor plan using automated techniques, such as logic grouping, physical partitioning, aspect-ratio assignment, pin optimization, block and cell placement, and routing estimation. Physical-floor-planning tools are fast because they take a global view of a design's physical implementation. They also allow you to quickly explore floor-plan options to find the best layout for your design. The floor plan provides the basis on which the other analysis and implementation tools of the design planner operate.

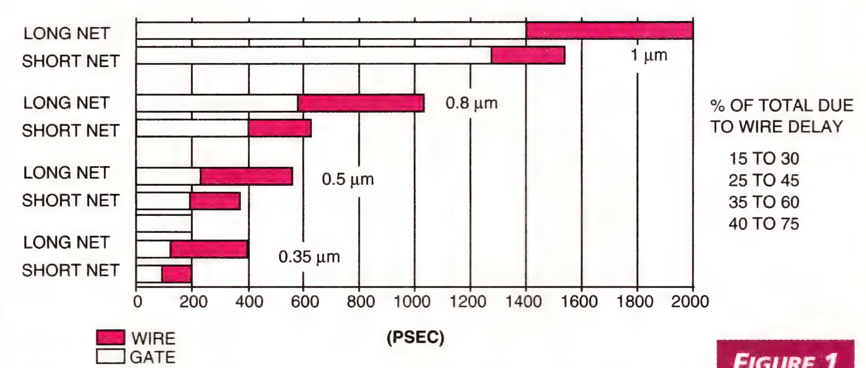


FIGURE 1

Gate delay has decreased by about 30% with each new process technology, but interconnect delays have not fallen as quickly. For 0.5-µm technologies, interconnect causes 50% of the delay.

Accurate delay prediction

Design tools can accurately predict delays using a floor plan as a base (**Fig 3**), but the first-order effects of deep-submicron processes require new delay-calculation methods. Further, deep-submicron ICs can handle shorter clock cycles, requiring greater accuracy than previous designs.

To accurately account for input slew and gate loading, cell libraries should provide nonlinear table models to cal-

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DEEP-SUBMICRON ASIC DESIGN

culate gate-propagation delay. The delay calculator must also consider the increase in resistance per micron of interconnect in deep-submicron designs. Increased interconnect resistance may affect both the load a driving gate sees and the pin-to-pin interconnect delay. Closer interconnects and greater use of multilayer interconnect technologies cause an increase in coupling and interlayer capacitance, which also affect delay. Failure to consider these deep-submicron effects can cause significant prediction errors (**Fig 4**).

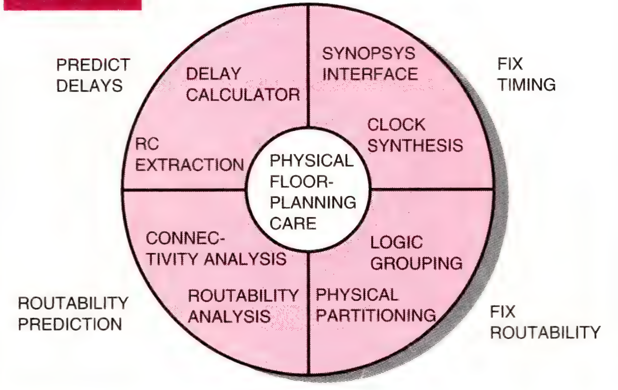
After full placement and routing, most physical designers accurately predict delays if they have considered deep-submicron effects. In logic-design, however, current tools and methodologies often predict delays with errors exceeding 100 to 200%. The inaccuracy results from the widespread use of statistical wire-load models. As a result, you may waste time optimizing a design if you base your optimizations on bad delay information. You may also fail to discover major timing problems until very late in the design cycle. Inaccurate delay predictions commonly cause designers to identify the wrong critical paths and spend a significant amount of time optimizing them. The designer then finds—after physical implementation—other paths that are more critical than previously optimized paths. As a result, the design fails.

Design planners for logical design resolve these problems without the time and expense of full detailed placement and routing. Design planners consistently predict delays to within a maximum error of 15% of the actual delay for short nets and 25% of the actual delay for long nets. Overall prediction accuracy is even better when you average it over most of a design's nets.

Fixing timing problems

Once you arm yourself with accurately predicted delays, identifying legitimate timing problems becomes relatively straightforward. Timing analysis and timing simulation examine the efficiency of a design. But, fixing timing problems is still difficult unless you use new tools and methodologies. The ability to back-annotate accurately predicted delays early in the design cycle is the first step toward faster and easier resolution of timing problems. With greater delay-prediction accuracy, synthesis tools do a better job of timing optimization.

FIGURE 3



Floor-planning is one of a design planner's key technologies.

FIGURE 4

DESIGN PROCESS	DELAY PREDICTION (%)	INCREASED TIME TO PRODUCE ESTIMATE
HDL ENTRY	TYPICAL ±100 TO 200	↓
SYNTHESIS		
DESIGN PLANNING	MAXIMUM ±15 TO 25	
PLACE AND ROUTE	MAXIMUM ±4	
SPICE	≤ ±1	

Design planners allow you to predict delays with a maximum error of 15 to 25% so that you can isolate timing problems earlier in the design cycle.

Incremental-optimization techniques, such as critical-path re-synthesis and in-place optimization, help solve timing problems. Critical-path re-synthesis provides a mechanism to reoptimize a critical path and its surrounding logic without affecting other parts of a design. In-place optimization allows you to increase buffer sizes to improve the timing on a path or to decrease buffer sizes to reduce area and power.

Other steps include back-annotation of the physical hierarchy to resolve problems through incremental synthesis. This technique is an important improvement because a design's logic hierarchy often is not the best one for meeting chip timing and size constraints, especially for large, complex designs. Not surprisingly, logic designers organize their hierarchy to match how a design functions. An optimum physical hierarchy, on the other hand, minimizes the number of connections between hierarchy blocks and maximizes the connections internal to a block. Without the ability to back-annotate physical hierarchy, you lose a major design strategy for improving a design's performance and routability.

By rapidly iterating between synthesis and design-planning tools, you can quickly and accurately resolve timing problems. Resolving these problems early means that you can avoid multiple placement-and-routing iterations later (**Fig 5**).

Predicting and improving design routability

Determining the routability of a design is critical to predicting an IC's size and performance. Today's ASIC-design tools use relatively simple calculations based on total cell area and number of nets to estimate design size. However, the estimates do not consider the increasing routability problems of deep-submicron designs. As a result, predictions

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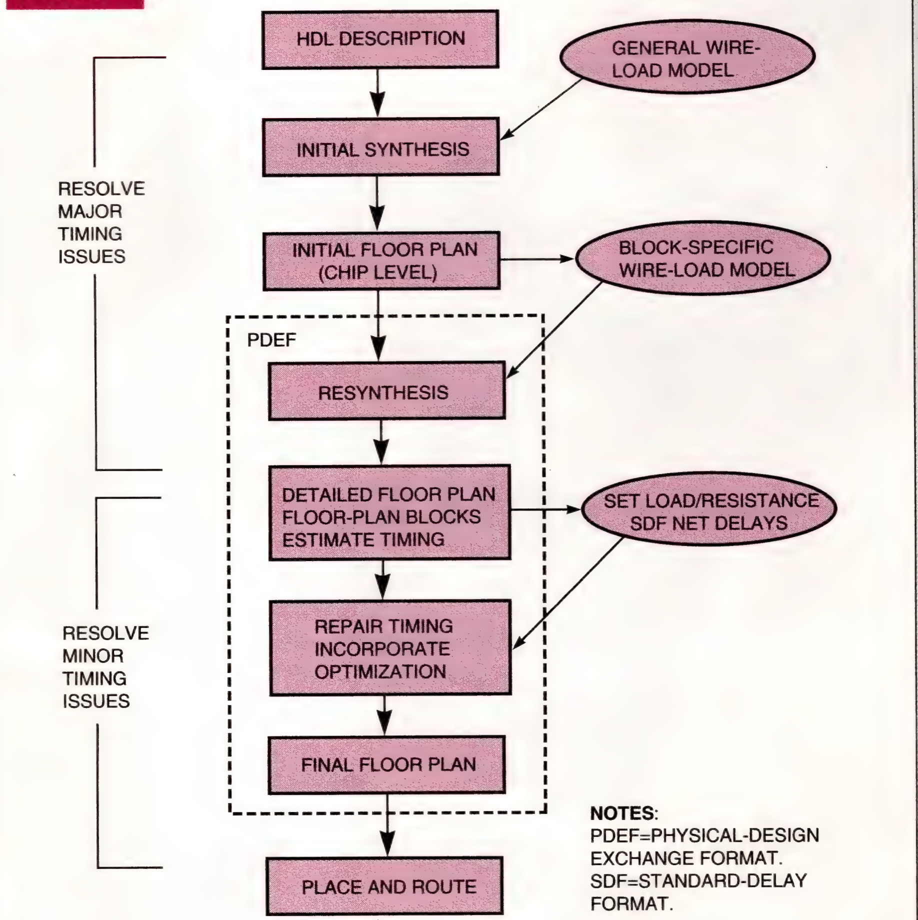
from these calculations are inaccurate and cause surprises late in the design cycle.

Design routability is a problem for many reasons. One reason is the continued explosion in design complexity. Designs have more cells and nets to place and route. A second reason is the use of top-down design methodologies employing synthesis tools. Logic synthesis increases the average number of connections per net 50 to 100%, creating increased congestion throughout the chip. A third reason is the increased number of macro blocks or megacells with many input and output pins, causing increased congestion. Finally, the use of larger buses causes problems for routers. You may consider one or more of these issues to accurately determine the routability of a design.

Fixing routability problems is difficult. Most place-and-route tools operate on flattened designs, so it is difficult to isolate routability problems and incrementally fix them early in the design cycle. In addition, because place-and-route tools typically flatten design hierarchy before they place and route, they generally cannot take advantage of the highly structured nature of a logic hierarchy. As a result, resolving routability issues requires several iterations and a lot of time.

FIGURE 5



By iterating between design planning, synthesis, and timing-analysis tools, you can identify and resolve problems early in the design cycle where they are least expensive to fix.

The use of design planners considerably improves the situation because they allow you to analyze a design for routability, to identify problems, and to resolve them. For example, automatic logic grouping and physical partitioning algorithms analyze a logic hierarchy and determine which portions of the hierarchy are well-structured for physical implementation and which are unstructured. You must further process unstructured portions to avoid routability problems. Automatic physical partitioning and regrouping algorithms then operate on the unstructured logic to repartition the design for physical implementation. Automatic floor-plan optimization, including block aspect-ratio optimization and pin-location optimization, also helps solve routability issues.

By introducing design planning into logical design, you can improve the performance and size of a design, and, by eliminating lengthy placement-and-routing iterations, you reduce design-cycle times. EDN

Author's biography

Bob Wiederhold is executive vice president and chief operating officer of High Level Design Systems, a company specializing in submicron IC-design tools. Previously, Bob spent nine years at Cadence Design Systems Inc, where he held senior management positions in the company's systems, ASIC, and IC businesses. Bob also spent five years as an IC designer at AT&T Bell Laboratories. He has an MSEE from Cornell University, Ithaca, NY.

Low-Power Single-Supply ICs

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CONTENTS

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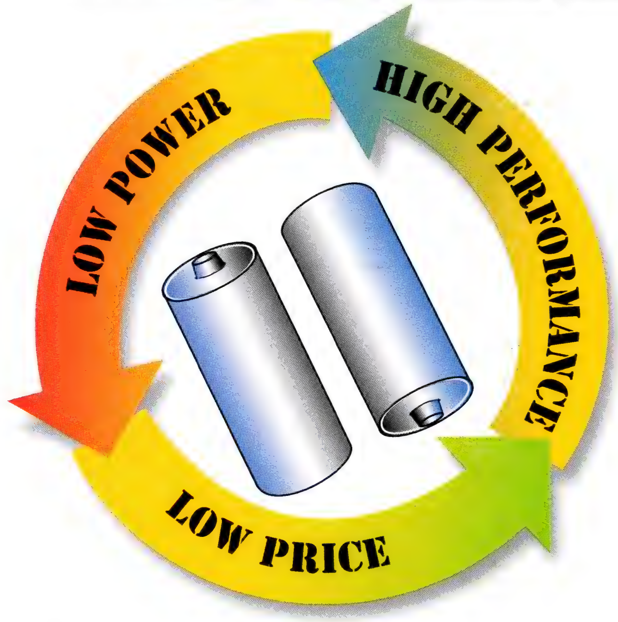


New Battery-Compatible 12-Bit ADCs Eliminate System Errors

When portability and performance are your design requirements, the only choice is the AD7853 or AD7858. With throughput rates up to 200 kSPS and a power dissipation as low as 4.5 mW, these converters are ideal for a wide variety of battery-powered and low-power applications, ranging from portable personal computers to instrumentation and control systems. The single-channel AD7853 and eight-channel AD7858 accept bipolar and unipolar input voltages and operate from power supplies ranging from 3 V to 5.5 V.

Both devices feature a calibration mode to null system offset and gain errors associated with external signal conditioning circuitry. The AD7853 and AD7858 are fully specified for ac and dc applications. INL is guaranteed (<1 LSB) and SNR is 70 dB. These devices feature a 24 µW (@ 3 V) power-down mode and flexible serial interface to accommodate three-wire SPI or two-wire 8051-compatible connections.

Two throughput rate versions (100 kSPS and 200 kSPS), are available in 24-pin DIP, SOIC and SSOP packages. Operating temperature range is –40°C to +85°C.

AD7853L	Price $6.45	Faxcode 1814	Circle 1
AD7858L	Price $6.95	Faxcode 1815	Circle 2

†All prices shown in USD, 1,000s, recommended resale, FOB USA

SINGLE-SUPPLY, LOW-POWER ANALOG-TO-DIGITAL CONVERTERS

New!

16 Bits in 16 Pins – $6.00

The AD7715, a complete transducer interface ADC for low-frequency measurement applications, offers 16 bits of resolution for only $6. It's ideal for use in portable instrumentation because it requires less than 0.5 mA of total supply current and features a power-down (maximum 50 µW) stand-by mode.

Unlike competitive devices, the AD7715's low power consumption does not reduce functionality. The AD7715 offers a programmable-gain front end with four gain settings (1, 2, 32 and 128), accepts differential inputs, and operates from either 3 V or 5 V supplies. The 3 V version is fully specified down to 2.7 V. Via the input serial port, gain settings, signal polarity and update rate selection can be easily configured in software. And the AD7715 improves design efficiency. Its three-wire serial interface reduces the number of interconnect lines and opto-couplers normally required for isolated systems.

The AD7715 is available in a 16-pin DIP and SOIC, and is specified over the –40°C to +85°C temperature range.

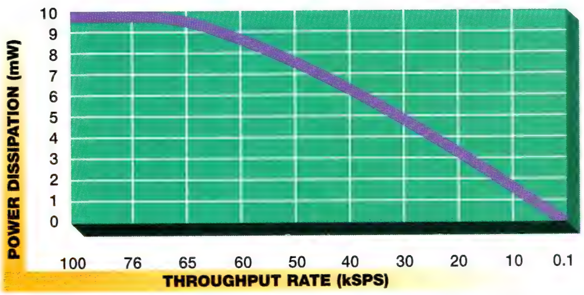
KEY FEATURES
- 50 µW stand-by mode
- 0.5 A supply current
- 3 V and 5 V operation

AD7715 Price $6.00 Faxcode 1813 Circle 3

New!

12-Bit ADC in 8-Pin SOIC Features Automatic Power-Down

When designing with the AD7896, smaller is better. The 12-bit AD7896 packs an 8-µs ADC, track-and-hold amplifier, control logic, and a high-speed serial interface, all in an 8-pin SOIC or DIP. Features of this tiny powerhouse include a proprietary *automatic power-down mode* invoked between conversion cycles, which makes it an efficient solution for battery-powered or portable applications. A high sampling rate mode is available as well. Power dissipation is 15 mW at full speed and only 36 µW in power-down mode. It accepts an analog input range of 0 to V_{DD}, operates from a single 3-V to 5-V supply, and consumes just 10 mW of power.



Many ac and dc accuracy specifications are guaranteed, including linearity, full-scale and offset errors, and dynamic performance parameters such as harmonic distortion and SNR.

AD7896 Price $6.75 Faxcode 1816 Circle 4

New!

Charge Balancing ADC for Low-Frequency Measurement Applications

The AD7714 is a complete analog front end for low frequency measurement applications. It combines high resolution and low power consumption with a five-channel programmable-gain front end to reduce external signal conditioning components. The AD7714 is completely under software control, with gain settings, signal polarity, filter cut-off, calibration and channel selection, all configurable using the input serial port.

This flexible component is perfect for use in smart, microcontroller- or DSP-based systems. It features a serial interface which can be configured for three-wire operation, and typically draws 1 mW in normal operation.

No missing codes ensures true, usable 24-bit dynamic range coupled with accuracy of 0.0015%. Self-calibration and system-calibration options eliminate ADC and system gain and offset errors.

The AD7714 is available in a 24-pin DIP and SOIC, and is specified over the – 40°C to +85°C temperature range.

KEY FEATURES
- Fully programmable
- 3-wire serial interface
- <1 mW power draw

AD7714 Price $11.00 Faxcode 1812 Circle 5

FOR DATA SHEET FAX BACK 1-800-446-6212

SINGLE-SUPPLY, LOW-POWER ANALOG-TO-DIGITAL CONVERTERS

12-Bit ADC Runs from 3-V Supply with Parallel Interface

The AD7883 is a fast, low-power 12-bit ADC with fully specified operation from a single 3-V power supply. Packaged in a 24-pin DIP or SOIC, the device contains a 15 µs successive-approximation ADC, on-chip track-and-hold amplifier and high-speed parallel interface. It features a 50 kSPS throughput rate and dissipates only 8 mW in normal operation, and a power-down mode which cuts consumption to 1 mW. The AD7883's reference input can be connected to V_{DD} for ratiometric measurements.

The AD7883 is guaranteed for supply voltages between 3 V and 3.6 V, and it's perfect for low-power and battery-powered applications where a complete 12-bit ADC solution is necessary for full-power signals up to 25 kHz.

The AD7883 is available in 24-pin DIP and SOIC packages. Operating temperature range is –40°C to +85°C.

KEY FEATURES

- Fully specified at 3 V
- High-speed parallel interface

AD7883 Price $6.95 Faxcode 1378 Circle 6

Fast 10-Bit ADCs Offer Simultaneous Sampling on Two Input Channels

The single-channel AD7776, dual AD7777 and octal AD7778 are a family of high-speed 10-bit sampling ADCs. The AD7777 and AD7778 allow simultaneous sampling on any two inputs. All three ADCs operate from a single 5-V supply and achieve throughputs up to 400 kSPS while consuming only 75 mW max of power under normal operation. A power-down mode is available for reduced power consumption to 7.5 mW.

The input signal range is $V_{BIAS} \pm V_{SWING}$, allowing users to tailor input ranges to match the application. They can also operate in the analog input range between 0 V to REF_{IN}.

The AD7776 is packaged in a 24-pin SOIC, the AD7777 in either 28-pin DIP or SOIC; and the AD7778 in a 44-pin PQFP. All parts are specified from –40°C to +85°C.

KEY FEATURES

- 400 kSPS throughput
- 2-channel simultaneous sampling
- Parallel interface

AD7776 Price $7.06 Faxcode 1351 Circle 7

AD7777 Price $8.29 Faxcode 1351 Circle 8

AD7778 Price $9.10 Faxcode 1351 Circle 9

SINGLE-SUPPLY ADCs

Model	Resolution (Bits)	Multiplex Capability (Channels)	Supply Voltage (V)	Input Range 0 to (V) or (± V)	Output Format (Ser/Par)	Reference Ext/Int (V)	On-Chip SHA	Power (mW, typ)	Conversion Speed (kSPS)
AD775	8	1	5	2	Parallel	Ext	Y	60	20000
AD7776/7/8	10	1/4/8	5	2	Parallel	Ext/Int	Y	50	400
AD7883	12	1	3.3	V_{DD}, $\pm V_{DD}$	Parallel	Ext	Y	9	50
AD7896	12	1	2.7, 5.5	V_{DD}	Serial	Ext	Y	9 (2.7 V)	100
AD7853/L	12	1	3.3, 5	V_{DD}	Serial	Ext & Int	Y	12/4.5 (3.3 V)	200/100
AD7858/L	12	8	3.3, 5	V_{DD}	Serial	Ext & Int	Y	12/4.5 (3.3 V)	200/100
AD7893	12	1	5	±10, 2.5	Serial	Ext	Y	25	117
AD7890	12	8	5	±10, 2.5, 4.096	Serial	Ext/Int	Y	50	100
AD7891	12	8	5	±10, ±5, ±2.5, 2.5, 5	Parallel	Ext/Int	Y	75	500
AD7892	12	1	5	As above	Parallel	Ext/Int	Y	60	600
AD7715	16	1	3, 5	20 mV, 2.5, ±20 mV, ±2.5	Serial	Ext	N	1.2 (3.3 V)	0.5
AD7714	24	1	3, 5	As above	Serial	Ext	N	1.2 (3.3 V)	1

Low-Cost Dual and Quad Op Amps Outperform CMOS Versions

The low-cost dual OP292 and quad OP492 single-supply op amps outperform comparably priced CMOS devices. These 4-MHz, 4-V/µs amps combine the attributes of complementary bipolar—precision and output drive capability—with the low cost of CMOS devices that consume less power. With 5-V supplies, the OP292 guarantees 800 µV offset over our new HOT temperature range (–40°C to +125°C), at no additional cost.

Input voltages can swing well below ground with output swings to ground. Current draw is less than 1.4 mA per channel for multichannel battery-powered applications. Both amps feature low voltage and current noise (15 nV/√Hz and 0.7 pA/√Hz) and 100 dB channel separation at 1 kHz. Applications include disk drives, mobile phones, multichannel industrial and servo control systems, modems, fax machines, pagers, and power supply monitoring circuits. Packaging options: 8- and 14-lead plastic DIPs or surface-mount narrow-body SOICs.

KEY FEATURES
- 15 nV/√Hz noise
- <800 µV offset
- High output drive

OP292	Price $1.00	Faxcode 1697	Circle 10
OP492	Price $1.63	Faxcode 1697	Circle 11

New!

Single-Supply FET-Input Op Amps Operate from +3 V to +36 V

The AD820 (single), AD822 (dual) and AD824 (quad) precision, low-power, FET-input op amps operate from a single 3- to 36-V range or from dual ±1.5-V to ±18-V supplies. Voltage outputs swing to within 10 mV of either rail-to-rail with inputs that can fall 0.2 V below ground. Their JFET input stage offers low bias current (≤10 pA at +25°C, B grade), and low offset errors over temperature (–40°C to +85°C) and 25 nV/√Hz noise at 10 Hz.

Quiescent current drain is only 620 µA, and both devices will drive loads up to 15 mA and 350 pF. They feature a unity-gain bandwidth of 1.8 MHz with 3 V/µs slew rate. Three-volt versions are optimized for low-power operation at no extra cost. The AD820 and AD822 are available in 8-pin plastic DIP and SOIC; the AD824 is packaged in 16-pin DIP and SOIC.

KEY FEATURES
- V_{OUT} to within 10 mV of rails
- 25 nV/√Hz noise
- 620 µA current drain

AD820	Price $1.28	Faxcode 1406	Circle 12
AD822	Price $2.04	Faxcode 1406	Circle 13
AD824	Price $3.38	Faxcode 1810	Circle 14

SINGLE-SUPPLY AMPLIFIERS

Model	Channels	Power Supply Range (V)	V_{IN} Range LL/UL (V)	V_{OUT} Swing LL/UL (V)	Supply Current per Amp (mA), max	V_{OS} (mV), max	I_B (nA), max	Band-width (MHz)	Current Output Drive (mA), min	SPICE Model (Y/N)
OP22	1	3 to 30	0/3.5	.8/4.2	0.0125	0.3	5	0.25	-	N
OP279	2	4.5 to 12	0/5	.075/4.8	3.5	4	300	5	45	N
AD820/2/4	1/2/4	3 to 36	0.2/4	.007/4.986	0.8	0.4	0.01	1.8	15	Y
OP183/283	1/2	3 to 36	0/3.5	.075/4	1.5	0.3	600	5	25	Y
OP291/491	2/4	2.7 to 12	0/5	.05/4.95	0.3	1	79	3	8	Y
SSM2135	2	4 to 36	0/4	.0035/4.1	2	2	750	3.5	30	N
OP292/492	2/4	4.5 to 33	0/4	.45/3.8	1.2	0.8/1	700	4	8	Y

SINGLE-SUPPLY, LOW-POWER AMPLIFIERS

Industry's Fastest 3-V Rail-to-Rail Op Amps Offer Guaranteed Performance

If your 3-V system needs ≥1 MHz gain bandwidth product, consider the OP183 and OP283. They combine 5 MHz bandwidth and low noise for use in low-voltage applications, such as ADC buffering, filtering, servo control and audio for portable computers.

These amps are thoroughly specified for operation at 3 V, 5 V and ±15 V. Unlike competing 3-V devices that specify only typical performance characteristics, the OP183 and the OP283 guarantee low offset, high gain, and input and output ranges that include ground. Noise is only 10 nV/$\sqrt{\text{Hz}}$, either amplifier can sink and source 25 mA—even with a 3-V supply. Both devices operate from −40°C to +85°C and are available in 8-lead plastic DIPs and SO-8 packages.

KEY FEATURES

- 5 MHz bandwidth
- 3, 5 and ±15 V
- 10 nV/$\sqrt{\text{Hz}}$ noise

OP183	Price $1.42	Faxcode 1675	Circle 15
OP283	Price $2.15	Faxcode 1675	Circle 16

New! Rail-to-Rail, High-Output-Current Op Amp Can Sink/Source ±80 mA

This single-supply dual rail-to-rail op amp is perfect for general purpose and audio signal conditioning where high current and capacitive load drive is crucial. The OP279 can sink and source currents of ±80 mA (typ) and drive capacitive loads up to 10 nF with full stability. For low-noise wideband audio amplification, the OP279 provides a 5 MHz bandwidth and 3 V/µs slew rate with <0.01% THD and 21 nV/$\sqrt{\text{Hz}}$ noise. Single-supply voltage inputs can range from 4.5 V to 12 V with guaranteed output performance. Current draw is less than 3.5 mA per amplifier. The OP279 is available in 8-pin plastic DIPs and SO-8 packages specified over the HOT (−40°C to +125°C) temperature range.

KEY FEATURES

- High current/capacitive drive
- <0.01% THD, 21 nV/$\sqrt{\text{Hz}}$ noise
- Low power consumption

OP279	Price $1.31	Faxcode 1811	Circle 17

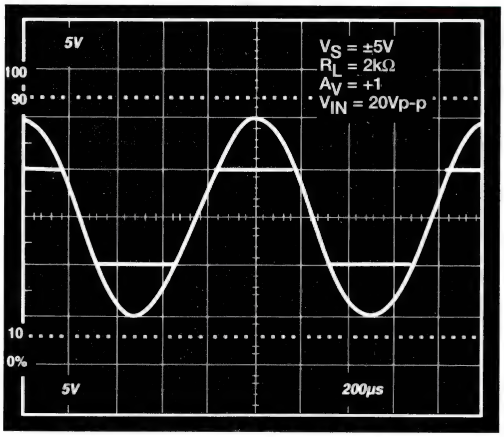
New! Rail-to-Rail I/O Op Amps Combine µPower Operation, Wide Bandwidth, High Accuracy

Three single-supply op amps combine "true" rail-to-rail input and output operation, low power consumption, wide bandwidth, and high accuracy. The single OP191, dual OP291 and quad OP491 operate from either a single 3-V to 12-V supply or ±5-V supplies and guarantee supply current below 350 µA (per amp) at 3 V; comprehensive specs are guaranteed at 3-, 5-, and ±5-V supplies. Output voltages can reach to within 50 mV of the positive rail and 10 mV of the negative rail and sink/source 13 mA.

The OP191, OP291 and OP491 protect against input overload by 10 V without output phase inversion or latch-up. They're ideal for low-power sensor and transducer interface systems that require the widest possible signal range and operate over the extended industrial (−40°C to +125°C) temperature range. The OP191 and OP291 are packaged in 8-pin plastic DIP and SO-8; the OP491 is housed in 14-pin DIPs and SO packages.

INPUT

OUTPUT



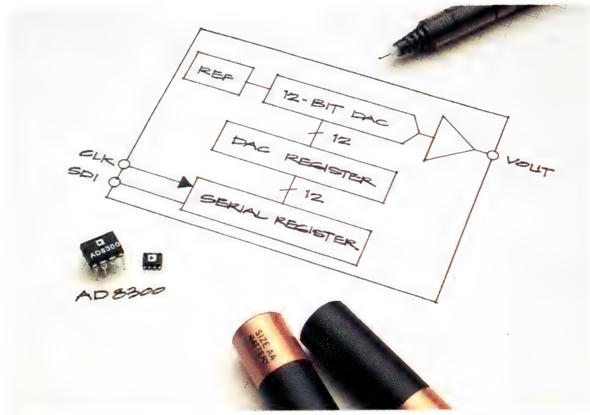
OP191	Price $1.62	Faxcode 1809	Circle 18
OP291	Price $2.16	Faxcode 1696	Circle 19
OP491	Price $3.23	Faxcode 1696	Circle 20

SINGLE-SUPPLY, LOW-POWER DIGITAL-TO-ANALOG CONVERTERS

Save Space, Power in PCMCIA Card Applications with World's First Complete 3-V 12-Bit DAC in SOIC

Until now you couldn't get a complete 12-bit DAC to operate from a single 3-V power supply. We've packaged this fully-trimmed device in a space-saving SO-8 to meet the critical 1.5 mm package height requirements of PCMCIA card applications and save board real estate. The AD8300 requires no external adjustments, and its fixed 0.5 mV/bit output scaling provides software-friendly programmability.

Characterization includes on-board reference specs to simplify your worst-case design analysis. The AD8300 is light on power too, consuming only 1.2 mA—operating from 5.5 V down to 2.7 V—to improve battery life in portable designs. The AD8300 features an easy-to-apply, three-wire serial interface and is available in 8-pin DIP and SO-8 packages specified from –40°C to +85°C.



KEY FEATURES
- Operates from 2.7 V to 5.5 V supplies
- Complete V_{OUT} DAC with internal reference
- 8-pin SOIC packaging

AD8300 Price $4.41 Faxcode 1808 Circle 21

Fast Octal/Quad 12-Bit DACs Cost $3/Channel

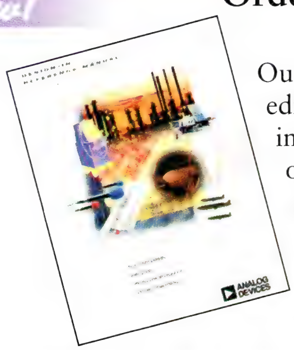
The quad AD7564 and octal AD7568 are 12-bit current-output DACs with independent reference inputs. They operate from a single 5-V supply voltage in normal mode, and 3.3-V to 5-V in biased mode. Both converters feature a fast serial interface for three-wire data loading with a 100 ns clock cycle time. Their low power dissipation (< 10 µW per DAC [AD7564]) makes them ideal for low-power, portable, and battery-operated equipment. Double-buffered latches allow the DACs to be individually addressed and simultaneously cleared or updated using asynchronous inputs, perfect for high pin-count ATE.

Both devices offer 0.5 LSB INL, 500 ns voltage settling with an AD843 op amp, and low (40 mVs) glitch impulse. The AD7568 is available in a 44-pin PQFP and the AD7564 is housed in a 28-pin SOIC, SSOP and DIP; both are specified for operation from –40°C to +85°C.

KEY FEATURES
- <10 µW power operation per channel
- 0.5 LSB INL
- Fast serial interface

AD7564	Price $11.90	Faxcode 1313	Circle 22
AD7568	Price $23.00	Faxcode 1314	Circle 23

Order Our New Design-In Reference Manual



Our latest one-volume edition contains an impressive 2,400 pages of data sheets, selection guides and a wealth of background information on converters, amplifiers, special linear products and support components. It covers everything from standard products to several hundred new ones for virtually every industry we serve. It's a thorough desktop reference for designing in today's most advanced signal processing solutions. To request your copy, simply complete and return the enclosed reply card.

Circle 35

FOR DATA SHEET FAX BACK 1-800-446-6212

Low-Cost Temperature Sensors Offer Complete and Programmable Thermostat Solution

Consider the AD22100 or TMP01 for your next temperature measurement and control application. The general purpose AD22100 provides on-board signal conditioning with a voltage output proportional to 22.5 mV/°C from –50°C to +150°C. The TMP01 contains its own 2.5 V reference and two matching comparators for easy programming of high and low trip points between –55°C and +150°C, V_{OUT} equals 5 mV/(°C + 273.15).

The AD22100 needs no external trimming, buffering or linearization circuitry, and its ratiometric operation offers an easy cost-effective solution for a/d converter and µProcessor interface. The AD22100 is available in TO-92 and SOIC packages.

The TMP01 eliminates the need for window comparators and buffer/drivers because its open collector outputs can sink 20 mA and drive control relays directly. The TMP01 is available in 8-pin plastic DIP, SO-8, and TO-99 metal can packages.

KEY FEATURES

- On-board setpoint control (TMP01)
- Ratiometric operation (AD22100)
- Free easy-design software

TMP01	Price $1.95	Faxcode 1807	Circle 24
AD22100	Price $0.98	Faxcode 1091	Circle 25

New! Five Voltage References Guarantee Precision Micropower Operation

These five new precision voltage references guarantee precision and micropower specifications. The REF192, REF193, REF194, REF195 and REF196 guarantee a 45 µA max quiescent current during normal operation, and less than 15 µA in sleep mode, perfect for low-power measurement applications and battery-operated instrumentation. The REF192, REF194, and REF195 guarantee <±2 mV output voltage error with 5 ppm/°C max tempco. The 3-V REF193 and 3.3-V REF196 guarantee less than ±10 mV initial accuracy error with 25 ppm/°C output tempco.

The REF192/3/4/5/6 family combines superb performance and full functionality. All references are available in 8-pin plastic DIP and SOIC packages specified for operation over the industrial temperature range of –40°C to +85°C. For use in automotive applications and extreme temperature conditions, performance characteristics are provided for operation up to +125°C.

KEY FEATURES

REF192	REF193	REF194	REF195	REF196
2.5 V	3 V	4.5 V	5 V	3.3 V

- Ultralow noise and dropout voltage
- Superb line/load regulation

REF19X	From $1.94	Faxcode 1761	Circle 26

World's First Quad SPST CMOS Switch is Fully Specified at ±5 V, +5 V, and +3.3 V

The ADG511, ADG512 and ADG513 contain four independently selectable quad SPST switches that operate from 3.3 V, 5 V or ±5 V. Ultralow power consumption (typically 0.5 nW) coupled with low ON resistance (<50 Ω), low leakage current (<100 pA) and fast switching times (t_{ON} < 35 ns; t_{OFF} < 150 ns) make these switches ideal for high resolution data acquisition systems and signal conditioning applications, as well as portable and battery-powered equipment.

These switches are fabricated on a trench-isolated process to prevent latch-up even with extreme overvoltage conditions. Trench isolation also limits the amount of leakage current: the ADG51X series offer a 25 pA typical leakage current. Guaranteed "make-before-break" operation allows interconnection between multiple outputs in multiplexer applications.

These parts are pin-compatible upgrades to Analog's ADG41X and ADG21X devices, available in 16-pin DIP, 16-pin SOIC and 16-pin cerdip, and specified over the industrial temperature range from –40°C to +85°C.

KEY FEATURES

- On resistance at 5 V
- Low leakage current
- 3 V & 5 V operation

ADG511	Price $2.04	Faxcode 1520	Circle 27
ADG512	Price $2.04	Faxcode 1520	Circle 28
ADG513	Price $2.04	Faxcode 1520	Circle 29

SINGLE-SUPPLY, LOW-POWER RS-232 TRANSCEIVERS

Multichannel RS-232 Transceivers Run 120 kB/s Data Rates

Today's portable computer and communications applications demand faster RS-232 throughputs. Three new, low-cost transceivers, the ADM202, ADM211 and ADM213, guarantee data rates up to 120 kB/s and use less power than competitive devices. Their high current output will drive extended cable lengths, providing you with improved throughput with greater design flexibility. The ADM202 is a pin-for-pin MAX202 replacement and requires only 0.1 µF 0805 body style capacitors—a 20¢ savings over conventional 1 µF designs—and guarantees less than 4 mA current draw.

The ADM211 and ADM213, also second sources (MAX211, MAX213), provide four drivers and five receivers with a low-power shutdown mode. These devices are designed specifically for battery-powered notebook computers, peripherals, modems and anywhere communications applications require 120 kB/s. The ADM202 is housed in a 16-pin DIP and SOIC. The ADM211 and ADM213 are available in 28-lead SOIC and SSOP.

KEY FEATURES

- 120 kB/s data rate
- Uses 0.1 µF capacitors
- 4 mA current draw

ADM202	Price $1.20	Faxcode 1528	Circle 30
ADM211	Price $1.85	Faxcode 1530	Circle 31
ADM213	Price $2.28	Faxcode 1530	Circle 32

Transceivers Provide Full RS-232 Levels from a 3.3 V Supply

Two improved second-source serial port transceivers are for portable computers, peripherals, printers and other battery-operated equipment. They can drive serial port mice and 116 kB/s data rates into 100-foot-long cables from a single 3.3 V supply. The ADM560 and ADM561 offer a maximum data rate of 120 kB/s, and exceed RS-232 standards with clean waveforms, even over a 100-foot cable. These devices require just 1.5 mA (5 mW) of power, and can handle up to 5 V digital inputs when working from a single 3.3 V supply without invoking protection diodes—perfect for split current applications.

The ADM560/561 feature an active high/low shutdown and enable sensor to further reduce power requirements during inactive operation. Both devices are available in 28-pin SOIC and SSOP packages, and are specified over the industrial temperature range from –40°C to +85°C.

KEY FEATURES

- Data rates up to 120 kB/s
- True RS-232 levels
- 1.5 mA current draw

ADM560	Price $1.80	Faxcode 1556	Circle 33
ADM561	Price $2.18	Faxcode 1556	Circle 34

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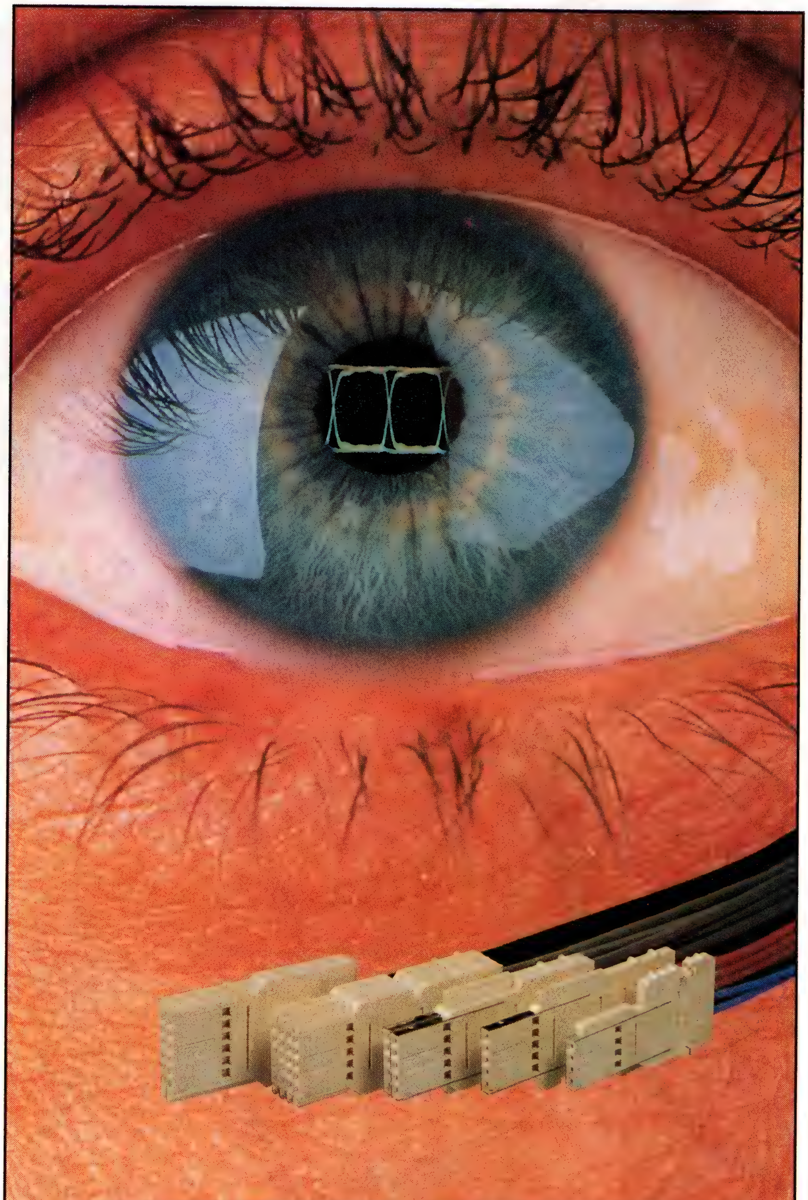

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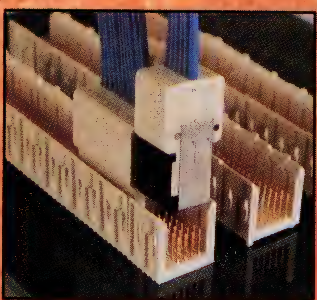

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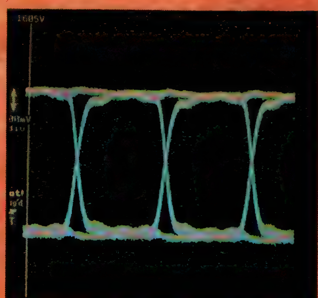

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CIRCLE NO. 88

Digital-servo and linear-regression methods test high-resolution ADCs

GREG WATERFALL AND BONNIE C BAKER, BURR-BROWN CORP

You've measured an ADC's differential linearity, but accuracy is difficult to obtain without compromising test time. Two new test methods can speed test time, even for high-accuracy ADCs.

The standard methods of measuring an ADC's differential linearity are most attractive for lab-bench testing or when measuring ADCs with resolutions less than 14 bits. Measuring higher resolution ADCs requires tests that can measure the required accuracy but that don't also result in long test time. A digital servo loop can measure an 18-bit ADC's differential linearity to a 16-bit level within 100 msec. Linear-regression techniques can measure 20-bit accuracy.

Both of these methods evolved from older tried-and-true test methods, such as those using an equivalent DAC, a triangle wave, and an oscilloscope. These methods are effective but time-consuming. The differential-linearity box method uses an equivalent DAC, a triangle-wave generator, a 3- or 4-bit reconstruction DAC, and an oscilloscope set in the X-Y mode. The oscilloscope displays a stair-step function, and each step represents the bit width of the indicated code. You visually measure the ADC's differential linearity from the scope display. This accurate but tedious method best suits ADCs that have conversion times shorter than 100 msec, such as successive-approximation converters.

The circuit in **Fig 1a**, for example, can display an eight-code segment of the transfer function of the ADC. The analog input voltage to the ADC, or device under test (DUT), is a summation of the input DAC's dc-output signal plus a triangle wave. The circuit sums these two signals using the OPA124 FET-input op amp in a transimpedance configuration. You can adjust the input DAC's logic input for the desired output. You can remove any offset and gain errors of the input DAC, triangle wave, and DUT using this DAC's offset and gain-adjustment options. The circuit latches the output of the DUT and connects it to a 3-bit DAC. The output of the 3-bit DAC connects to the vertical input of an oscilloscope. The triangle-wave input to the DUT connects to the horizontal input of the oscilloscope.

The transfer function of the 3-bit DAC produces an analog representation of the data output from the latches. In **Fig 1a**'s case, bits 11 and 12 of the ADC's 12-bit word determine the first 2 LSBs (least significant bits)of the 3-bit DAC. One of the remaining 10 bits in the word, which you select using the array of AND gates, drives the third and MSB (most significant bit) of the 3-bit DAC. In **Fig 1a**, bit 2 of the latched ADC output drives the MSB of the 3-bit DAC. At one-fourth of the converter's full-scale range, this MSB switches between 1 and 0. As **Fig 1b** shows, bits 11 and 12 of the 12-bit word count 00, 01, 10, 11, 00, 01, 10, 11, and so on, as V_{IN} increases. These input codes create the stair step in **Fig 1c**. The stair step comprises a cycle of four steps until the MSB of the 3-bit DAC changes from 0 to 1 at one-fourth full-scale range. At this point, the stair-step output of the DAC continues past the initial four steps and proceeds onto the next four steps, as the middle of **Fig 1c** indicates.

This setup allows you to see differential-linearity errors, missing codes, hysteresis errors, and noise on the scope screen. Differential-linearity error is the deviation from the ideal 1-LSB step size (see **box**, "ADC transfer-function basics revisited"). **Fig 2** shows the actual measurement results of two separate ADCs. The ADC in **Fig 2a** has a near-perfect transfer function, and the ADC in **Fig 2b** has a missing code at the MSB code carry. The differential-linearity error for **Fig 2b**'s converter is –1 LSB.

This test method works well for bench testing and engi-

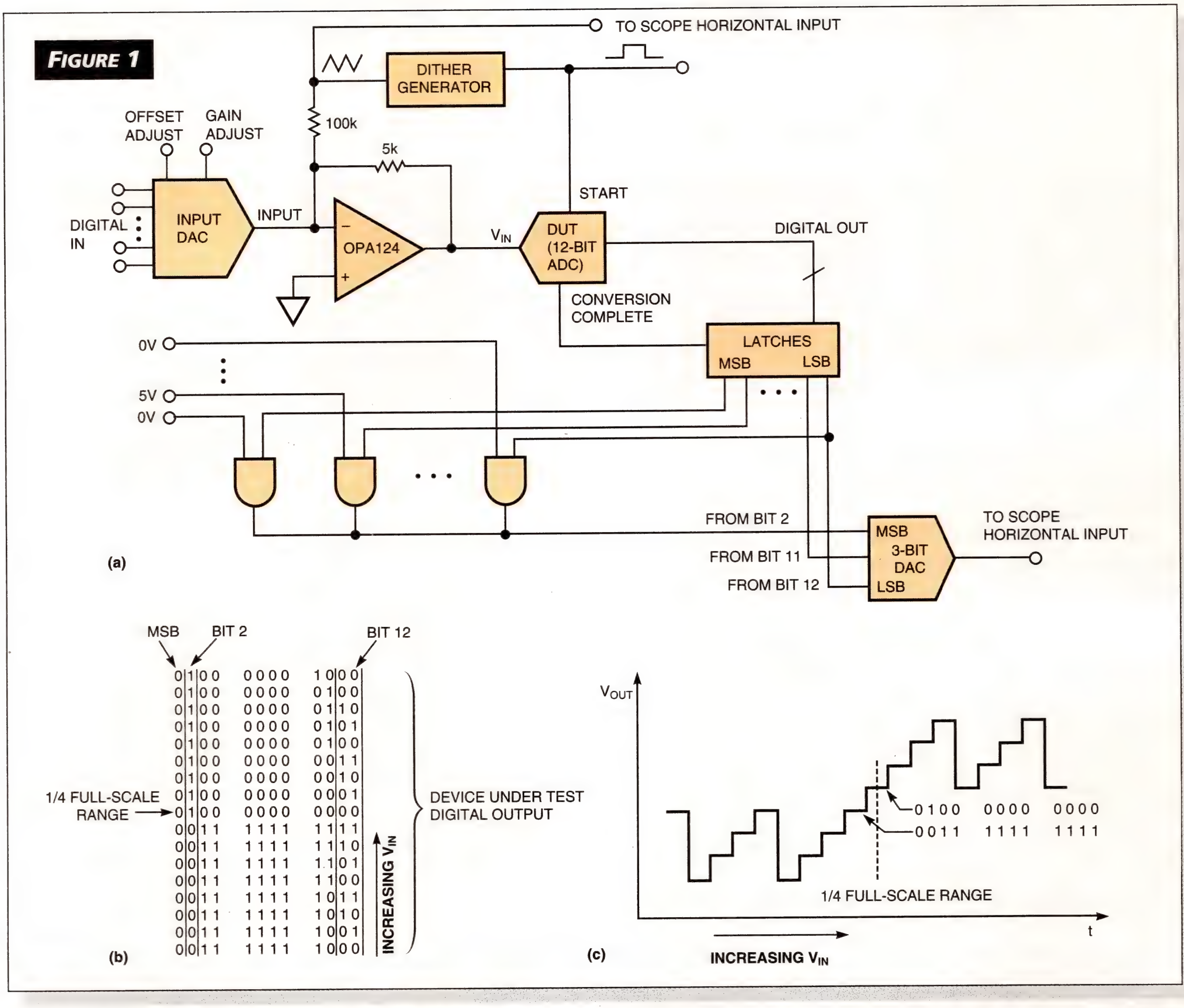
neering analysis, but, because it is slow and tedious, it does not suit production environments. Because you perform these tests manually, a single measurement may take several seconds to a minute, depending on the sophistication of the setup. Also, a converter's noise limits the test's accuracy.

For example, a 16-bit ADC with 1/2 LSB rms noise has a display similar to that in **Fig 3a**, a photo of a test using a 5-bit DAC. This "smearing" effect makes visual measurements difficult and inaccurate. The digital output of any 16-bit ADC represents the sum of internal noise of the device and the converted input signal. This noise is an artifact of the inherent noise in the circuit as well as the device noise of the converter.

You can easily observe this noise in a bar-graph format (**Fig 3b**). This graph records a series of conversions by the same 16-bit ADC with a constant dc input voltage. Repeated conversions of the same input voltage show that the ADC produces a distribution of codes because the inherent noise is larger than the quantization noise.

Analog servo loop speeds test time

As ADCs increase in resolution, they require techniques that allow accurate dc testing of higher resolution ADCs within reasonable test times. An analog-servo-loop test method (**Fig 4**) automates a differential-linearity test, which speeds test time compared with visual inspection. The test method uses an integrator, a digital comparator, and a DVM to measure the ADC's performance. During conversion, the DUT converts the analog voltage, V_{IN}, to a digital word. The test then compares this word to a predetermined digital



This tried-and-true ADC test method (a), which uses an input DAC, triangle-wave generator, and 3-bit reconstruction DAC, relies on visual inspection of the resulting stair-step function (c) on an oscilloscope. The ADC's digital output codes (b) drive the 3-bit DAC.

word, the "target code," that the code latch generates. If the digital output of the DUT is equal to or greater than the target code, the output of the comparator will be equal to 5V. Otherwise, the comparator's output is 0V.

The circuit converts the voltage at the output of the digital comparator to a current through R_1. Also, the circuit adds an offset current to the inverting node of the op amp through R_2 to allow for negative and positive input currents into the integrator. The circuit integrates the sum of I_1 and I_2 using C_1 and converts the result to a triangle wave at V_{IN}. Initially, C_1's role is to quickly bring V_{IN} into the proper range. The value of C_1 must be small enough to allow for quick changes in V_{IN} from one conversion cycle to the next. If C_1 is too large, the servo loop cycles through every code on the way to the code of interest. When measuring a 16-bit ADC at full scale, the test could cycle through 65,536 conversions before making a valid measurement.

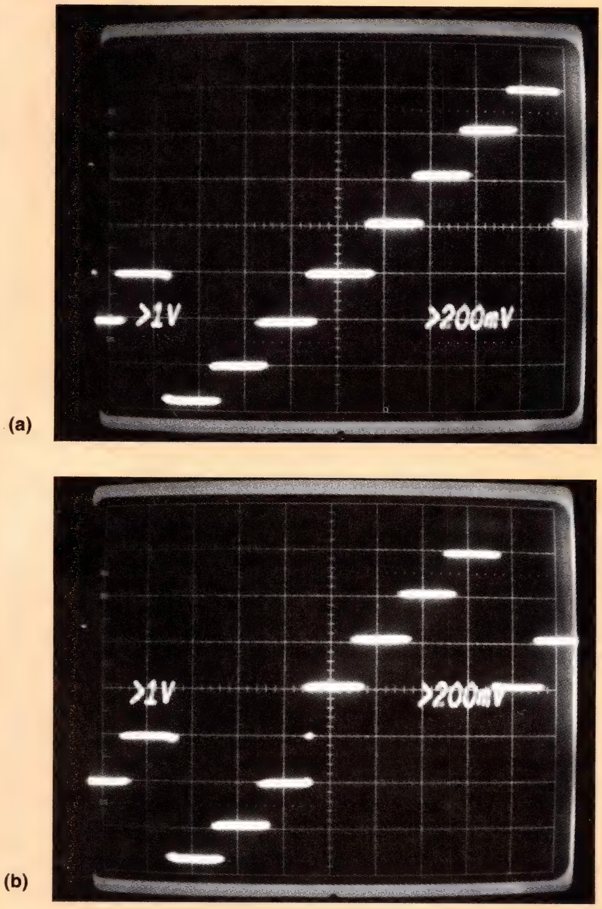
C_2, in parallel with C_1, completes the precision measurement. C_2 must be large enough to ensure that the output of the ADC toggles between 2 adjacent bits. If the output of the comparator is equal to 5V, the integrator output decreases in the negative direction. The converse is true for a comparator output voltage of 0V. The integrator output ideally is a triangle wave, centered on the transition voltage, with a peak-to-peak amplitude of

$$dV_{IN}=-I/(C_1+C_2)dt,$$

where dV_{IN} equals the peak-to-peak amplitude of the output of the integrator, C_1+C_2 is the integrator capacitor, I equals the integrator input current (I_1+I_2), and dt is the conversion interval. The DUT's noise and hysteresis, as well as asymmetrical integrator input currents, cause the integrator to deviate from the ideal triangle wave.

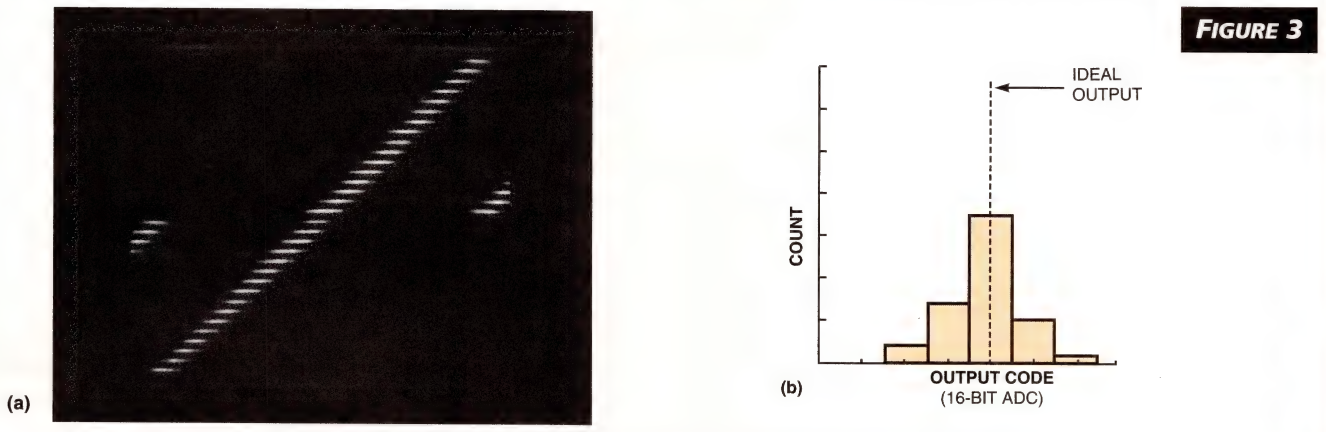
Simple RC lowpass networks filter the transition voltage that the DVM then acquires. The DVM further filters the output of the integrator by averaging the acquired voltage. The peak-to-peak amplitude of the triangle wave defines the resolution of the test and should be small (equivalent to 1/16 LSB

FIGURE 2



An ADC with a near-perfect transfer function (a) displays uniform code widths, but the ADC in (b) has a missing code at the MSB code carry.

FIGURE 3

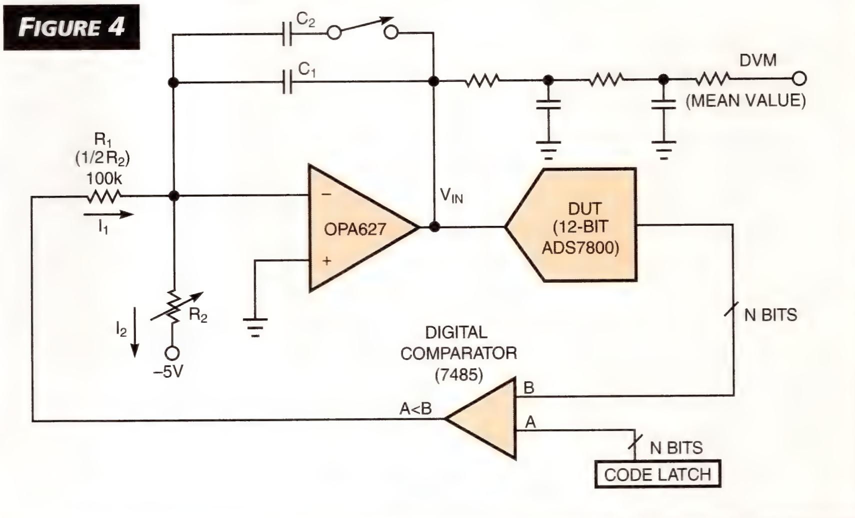


Using visual inspection to test 16-bit ADCs is difficult because of "smearing" effects (a). Multiple conversions of a higher resolution ADCs actually show a distribution of output codes around the ideal output because of noise in both the converter and the surrounding circuit.

or less). On each successive conversion, the test makes a new decision, and the input voltage to the ADC eventually stabilizes within an acceptable window, equal to dV/dt, that the integrator circuit determines.

The resulting DVM measurement represents the input voltage for a given bit transition. For target-code word N, the resulting DVM measurement is equivalent to the input voltage at the transition from code N–1 to code N. For any code word N, the differential linearity is simply the difference in the input voltages of the adjacent code transitions. For example, the differential linearity for code N is the change in voltage between the N–1 and N transition and the N and N+1 transition. The actual differential-linearity error is equivalent to this change-in-voltage measurement minus an ideal least significant bit.

FIGURE 4



An analog servo loop provides test automation and repeatability but has its drawbacks: The integrator is sensitive to noise and EMI, and interrupting the test for any reason can cause long delays.

The analog-servo-loop method offers the advantage of having infinite resolution because it is analog. This method provides a step toward automation and repeatability but has some problems. For instance, the analog meter must have at least 16-bit resolution. Problems can arise because of the sensitivity of the integrator to noise and EMI at the test sight. This method can be somewhat slow (although C_1 improves its speed) because of the search-and-wait time for the initial code and the averaging to obtain an accurate measurement. Finally, you can't easily stop the test because the op amp continually updates the ADC input voltage in relation to the comparator's digital input. However, with no conversion command, the ADC output doesn't change; thus, the comparator doesn't change, and, finally, the integrator's output voltage swings to a rail. To restart the test, you must wait for the servo loop to return to its proper operating point. The inability to easily stop the test becomes a problem when you're actively trimming the ADC or when you need to interrupt the test for another reason.

Digital servo loop further improves testing

A digital-servo-loop test method overcomes the analog approach's main deficiencies. The basic digital-servo-loop test method uses a digital comparator, an N-bit latch, an up/down counter, a DVM, some control logic, and a servo DAC (**Fig 5a**). In this test, the up/down counter and the servo DAC replace the integrator in the analog servo loop, which solves two of the problems of the analog method. First, the integrator in the analog servo loop is sensitive to noise and EMI, whereas the DAC in the digital-servo-loop test configuration is not. Second, you can easily stop the digital servo loop and hold it static during laser-trim procedures or for any other reason the test algorithm determines. The initialization of the analog servo loop can be tedious and time consuming, whereas you can easily program the desired test voltage for the digital servo loop into the up/down counter.

The control logic in the field-programmable gate array (FPGA) initiates a conversion of the DUT. The converted word appears at the input of the digital comparator, which compares the target code from the code latch to the output of the DUT. Based on the output of the digital comparator, the FPGA updates the up/down counter. The digital code sent to the DAC is either 1 bit higher or 1 bit lower than the previous conversion. The DAC uses this new code to produce a new analog output for the next conversion. In this manner, the circuit determines the transition voltage of the ADC to the level of accuracy that the DAC can produce. The DAC729 works well in this circuit because it is an 18-bit DAC, whereas the ADS7806 DUT is a 12-bit ADC. The servo DAC must be at least 2 bits more accurate than the DUT to ensure measurement accuracy. It may be difficult or impossible to find a DAC with high-enough accuracy to test higher accuracy ADCs.

As the test-requirement accuracy increases, **Fig 5a**'s digital-servo-loop test slows because of the required accuracy of the servo DAC's output. You can use averaging techniques to improve the repeatability of the measurement if the background noise levels are high. If the DUT is an 18-bit ADC, the test time can be several seconds. By adding an attenuation stage and a pedestal DAC to establish the operating point, the high-resolution DAC is no longer necessary, and the test time can decrease by a factor of 10 or more (**Fig 5b**).

In **Fig 5b**, the input to the DUT is the summation of a pedestal DAC and a servo, then multiplying, DAC. The test holds the pedestal DAC at a constant dc output during the measurement of a particular code. V_{REF} adjusts the multiplying DAC based on the servo DAC's output. The DUT converts the analog signal at V_{IN} to a digital code, which the digital comparator then compares to the target code. The comparator increments the up/down counter, which sends a new

ADC TRANSFER-FUNCTION BASICS REVISITED

The transfer function of an ideal, 4-bit, unipolar ADC (**Fig A**) shows the analog input signal on the horizontal axis and the digital output on the vertical axis. The first transition code occurs at an input voltage of ½ LSB, so that the center of each step occurs at the same voltage as the output of an ideal 4-bit DAC.

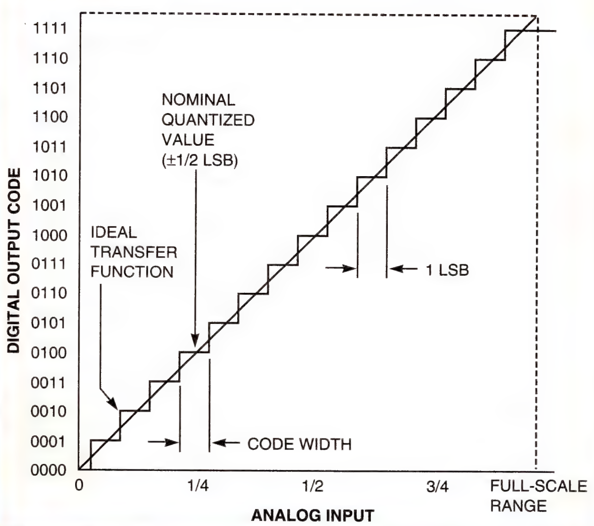
Each step of the transfer function is 1 LSB wide, and each digital output is valid over a range of input signals. The range of the analog input for a given output code is the width of the code. The width or range of uncertainty of the code, or quantizing error, is ideally ±½ LSB, which is inherent to all ADCs.

The first tests you typically perform on ADCs are for offset and gain error. Offset error is a consistent deviation from the ideal transfer function and appears to be a shift in the transfer function (**Fig B**). This error is likely to be the most prevalent error on the first transition. However, a correct measurement of offset error must also take gain error into account. As **Fig B** indicates, gain error appears as a change in the slope of the transfer function. To determine the gain error of an ADC, subtract the final transition voltage from the first transition voltage. By doing so, you also algebraically remove the offset error.

Gain and offset are not the most critical errors that determine an ADC's usefulness in most applications. You can usually calibrate out these errors using hardware or software. In contrast, differential and integral linearity are important specifications for most ADC applications because they represent irreducible errors.

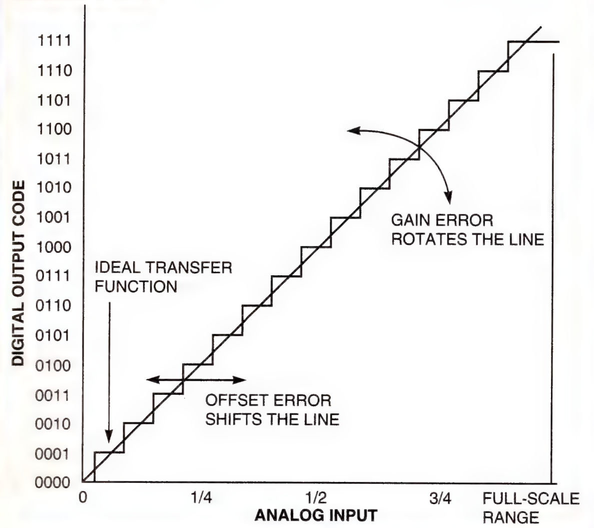
Fig C shows a nonideal transfer function of a 4-bit ADC, illustrating some examples of differential and integral errors. Differential nonlinearity is the difference between an ideal LSB code width and the actual code width. Integral nonlinearity (INL) is the deviation of the transfer function from the ideal straight line once you remove the offset and gain error.

FIGURE A



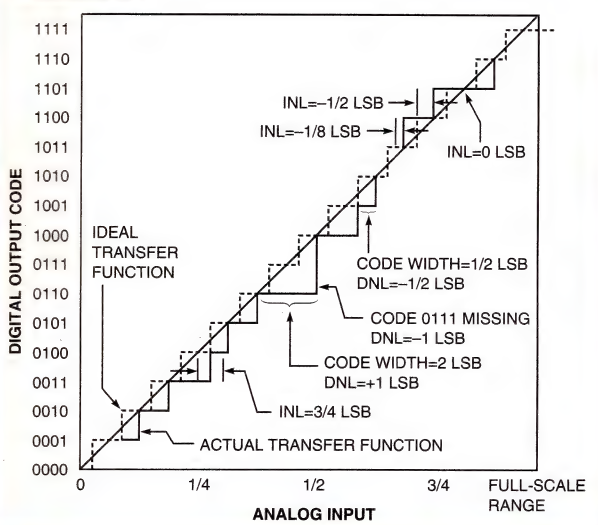
An ideal, 4-bit ADC has uniform code widths and follows a straight, diagonal line.

FIGURE B



ADC offset errors shift the ideal transfer function along the horizontal axis, and gain errors rotate the straight line.

FIGURE C



Differential- and integral-linearity errors appear in the ADC transfer function as nonuniform code widths and deviations from the ideal straight line, respectively.

code to the 12-bit servo DAC. The circuit further improves the output accuracy of the DAC7541 multiplying DAC by the ratio of R_1 to R_2. Now, the limiting test-time factors in this circuit are the DVM's low speed, the DUT's output noise, and the analog filter's settling time.

You can eliminate the DVM to speed test time even further without sacrificing measurement accuracy. By adding an accumulator and a digital divider (**Fig 6**), the differential-linearity measurement is accurate to a 16-bit level with a standard deviation of 0.1 LSB. In practice, this modified digital servo loop can test and trim an 18-bit ADC. The system measures differential linearity at the 16-bit level with a standard deviation of 0.1 LSB. The time for one measurement is less than 100 msec.

Increasing accuracy to 20 bits

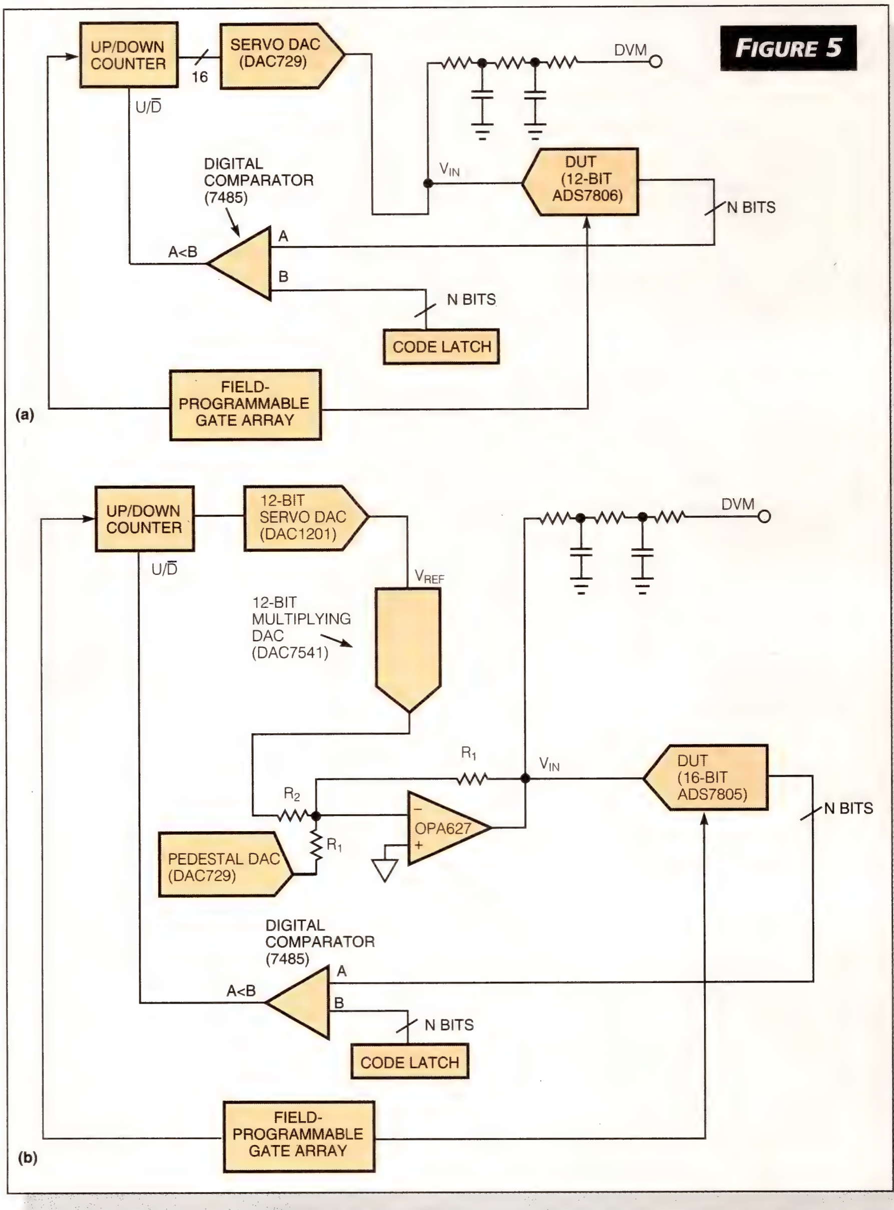
Despite the various improvements, all of these methods have difficulty testing accuracy as resolution increases beyond 18 to 20 bits. The DUT in **Fig 6** is the 20-bit DDC101. At this level, linear-regression techniques can accurately measure differential-linearity error. A linear-regression test measures multiple points near the bit transition and estimates other expected points around the transition. This test method actually requires the longest test time, but the method's accuracy is useful for testing state-of-the-art, high-resolution ADCs.

The simplest approach to using linear regression to determine differential-linearity errors is to measure two points of the converter that you know to be relatively accurate and extrapolate an "ideal" transfer function from these two points for the behavior of the remainder of the A/D. The test compares the ADC's actual measured performance to this "ideal," and the difference is the differential error of the converter. To complete this measurement, you determine which two points should you use to establish the "ideal" measurement reference that are above and below the measurement point of interest. You must also determine the converter's ideal voltage for 1 LSB.

The answer to the first question depends on the resolution of the converter and the desired final accuracy of the part. For example, on a 12-bit ADC with a desired final differential-linearity specification of ±½ LSB, you can choose the transition of N and N+1, where N is the code you want to measure. If the code width is 0, the measured differential-linearity error is –1 LSB; if the code width is 2, the error is +1 LSB.

As the resolution of an ADC increases, the allowable linearity error often increases more than you might expect. For example, many 16-bit ADCs provide 14-bit differential linearity. If you use the same test transitions as for the 12-bit ADC (N and N+1) to test a 16-bit converter, the test results will likely be incorrect. The 16-bit ADC may have a differential-linearity error of greater than –1 LSB, which the 16-bit ADC's specification allows, but the test still indicates a too-small and incorrect result of –1 LSB. For this reason, it is often

FIGURE 5



In this digital-servo-loop test (a), the up/down counter and the servo DAC replace the analog method's integrator, which reduces sensitivity to noise and makes it easier to start and stop the loop. To speed the testing of higher resolution ADCs, the circuit in (b) adds an attenuation stage and a pedestal DAC to replace the slower DAC729 with the 12-bit DAC1201.

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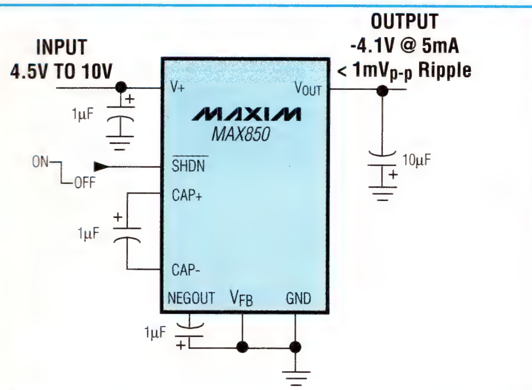

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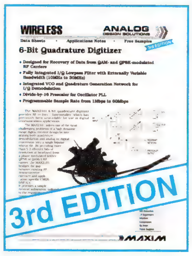

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ADC TEST TECHNIQUES

desirable to choose measurement points farther away from the transition of interest for higher resolution converters. For example, selecting a transition of N–4 and N+4 as the measurement points for a 16-bit ADC lets you measure errors as great as ±4 LSB.

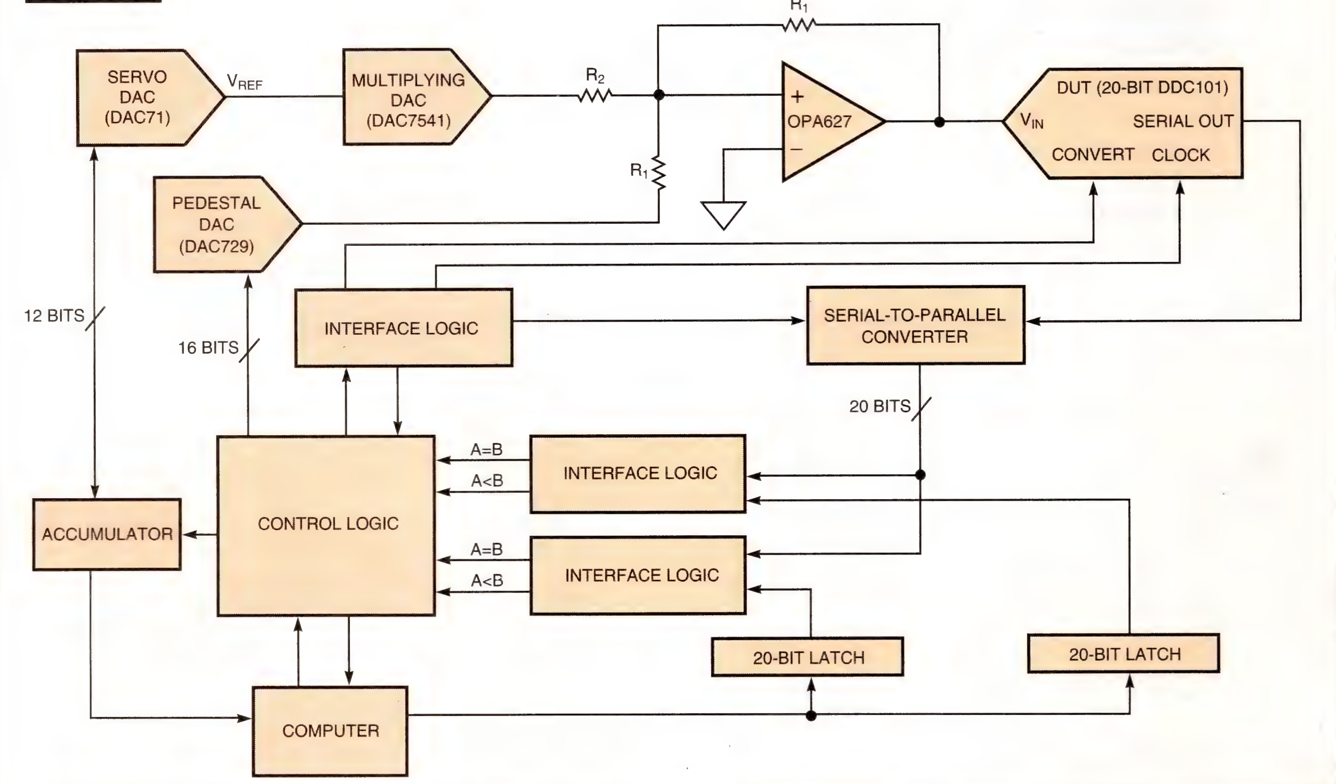
There are several possible answers to what a converter's ideal voltage for 1 LSB is. The simplest method of determining an ideal LSB is to measure the endpoints of the converter and divide by the number of codes in the converter. For example, a 12-bit ADC with ideal endpoints at 0 and 10V could have measured endpoints at 0 and 9.95V. This converter would have an LSB of 9.95V/(212–1), or 2.430 mV (the ideal LSB size is 2.442 mV). This approach removes gain error from the calculation. However, this gross calculation works only if the ADC is well-behaved; that is, its transfer function has only random errors and no large differential-linearity errors on the order of 2 or 3 LSB. If the converter is untrimmed or has a systematic error—an error that occurs in predictable places in the transfer function—this method provides incorrect results.

For example, if the converter has a systematic error such that every fourth bit transition has a +0.4-LSB error, using the endpoints to calculate 1 LSB yields a result that is 10%, or 0.1 LSB, too high. Another method is to measure a small portion, known to be almost ideal, of the converter's span You can then use this estimate as the ADC's ideal LSB to remove any problems of untrimmed or systematic errors. However, if this span is only around 10 to 20 codes, errors (around 1%) are likely because the measurement is so small.

For high-resolution ADCs, such as Burr-Brown's 20-bit DDC101, you must choose points far enough away from the transition that they aren't affected by any anomalies the differential-linearity error causes. The DDC101 is a precision, wide-dynamic-range, charge-digitizing converter that converts low-level currents, such as photosensor outputs, directly to digital words. Because the device is oversampling, it tends to smooth the differential-linearity error and distribute it across 100 codes of the converter's span. When testing the DDC101, choose the two points at least 50 codes away from the transition of interest. A 1% error in the LSB calculation can make an error in the differential linearity measurement of 100 LSB×1%=1 LSB, which may be unacceptable.

You can avoid the problems of determining the ideal LSB by using a more sophisticated linear-regression technique. For example, measure the points on the DDC101 that are 200, 150, 100, and 50 codes *below* the transition. From this data, draw a line and determine an expected input value for

FIGURE 6



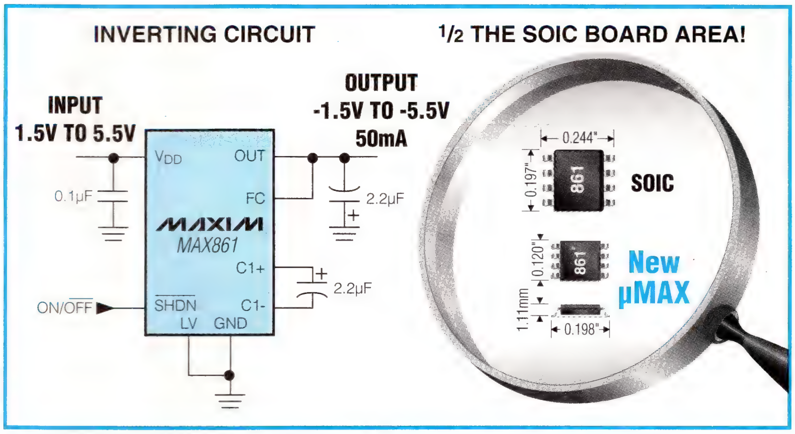
This modified digital servo loop can test and trim an 18-bit ADC and is the basis for linear-regression test techniques.

SMALLEST 50mA CHARGE-PUMP INVERTERS & DOUBLERS FIT IN 0.05in²

5-Times More Output Current and 1/2 the Area of '7660

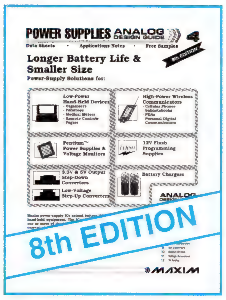
The MAX860 and MAX861 charge-pump DC-DC converters use no inductors and only small capacitors to invert or double their inputs. Use them to provide compact, inexpensive biases for LCD displays and other analog circuitry in battery-powered equipment. A high switching frequency and Maxim's new thin μMAX™ package allow the *entire circuit* to fit in less than 0.05in² (including external components). Switching frequency is selectable in ranges from 6kHz to 250kHz, allowing you to choose optimal capacitor size, current consumption, and output ripple frequency (i.e., above the audio range).

- **New μMAX™ Package**
  1.11mm High (max)
  0.024in² Area (max)
- **1.5V to 5.5V Input Range**
- **'7660 Pin-Compatible**
- **1μA Shutdown Current**
- **Low Output Impedance (12Ω)**
- **Selectable Switching Frequency**
  6, 50, 130kHz (MAX860)
  13, 100, 250kHz (MAX861)



The MAX860 and MAX861 provide more current and use less area than Maxim's industry-standard '7660. They have a higher switching frequency, lower output resistance, and smaller packages. The MAX860/MAX861 are pin-compatible with the '7660.

PRODUCT	PACKAGE FOOTPRINT (in² max.)	PACKAGE HEIGHT (mm max.)	SWITCHING FREQUENCY (kHz)	OUTPUT CURRENT (mA)	ROUT (Ω)	VOUT (V) (at VIN = 5V, IL = 50mA)
MAX860/861CUA (μMAX)	0.024	1.11	6 to 250	50	12	-4.4
MAX860/861CSA (SO)	0.048	1.75	6 to 250	50	12	-4.4
'7660CSA (SO)	0.048	1.75	10	10	55	-2.25



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CIRCLE NO. 118

ADC TEST TECHNIQUES

the point 50 codes *above* the transition. The difference between this ideal point and the actual measured point is the differential-linearity error of the code transition. Using this method, Burr-Brown measures and actively laser-trims the DDC101 to within ±0.5 ppm.

You can use the circuitry in **Fig 6** to perform a linear-regression differential-linearity measurement on a high-resolution converter. First, the control logic sets the multiplying DAC's input code so that the equivalent servo DAC's full-scale span is approximately 400 LSB at the DUT's input. The test then sets the servo DAC's input code to minus full scale and sets the pedestal DAC so that the DUT's input voltage is 250 LSB below the target code. During the rest of the measurement, the pedestal DAC's output voltage doesn't change. The DUT must perform a sufficient number of conversions to obtain a stable measurement, and the circuit stores the average of this output code. The test then increases the servo DAC's input code to create a 50-LSB increase in the DUT code and stores another output-code average. The test repeats this procedure for codes 150, 100, and 50 LSB below the target code.

From these five sets of servo-DAC input codes and DUT output codes, you can create a regression to estimate the correct output code for a servo DAC code 50 LSB above the DUT target code. You then set the servo DAC's input code to this value and average the DUT's output code. The difference between the predicted DUT output code and the measured output code represents the differential-linearity error of the target code, assuming all other code transitions within 250 DUT target codes are linear. EDN

Authors' biographies

Greg Waterfall is a test-engineering manager for Burr-Brown's Linear Division, Tucson, AZ, where he has worked for eight years. He is also managing a product-development group. Waterfall holds a BSEE from the University of California—Berkeley, Berkeley, CA, and an MBA from the University of Arizona, Tucson, AZ.

Bonnie C Baker is an applications engineering manager for the Components Division of Burr-Brown, Tucson, AZ, where she has worked for eight years. She has worked in various engineering capacities, including analog design, strategic marketing, applications, and production engineering. She received an MSEE from the University of Arizona, Tucson, AZ, and lists music as her main hobby; she plays a variety of instruments and has participated in orchestras, bands, and singing organizations.

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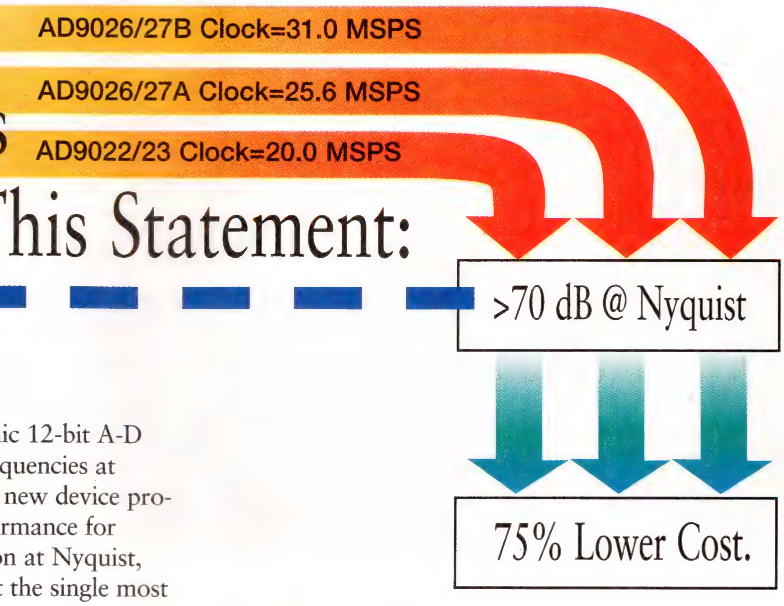

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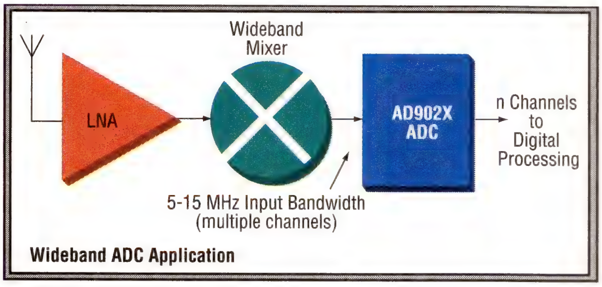

Wideband ADC Application

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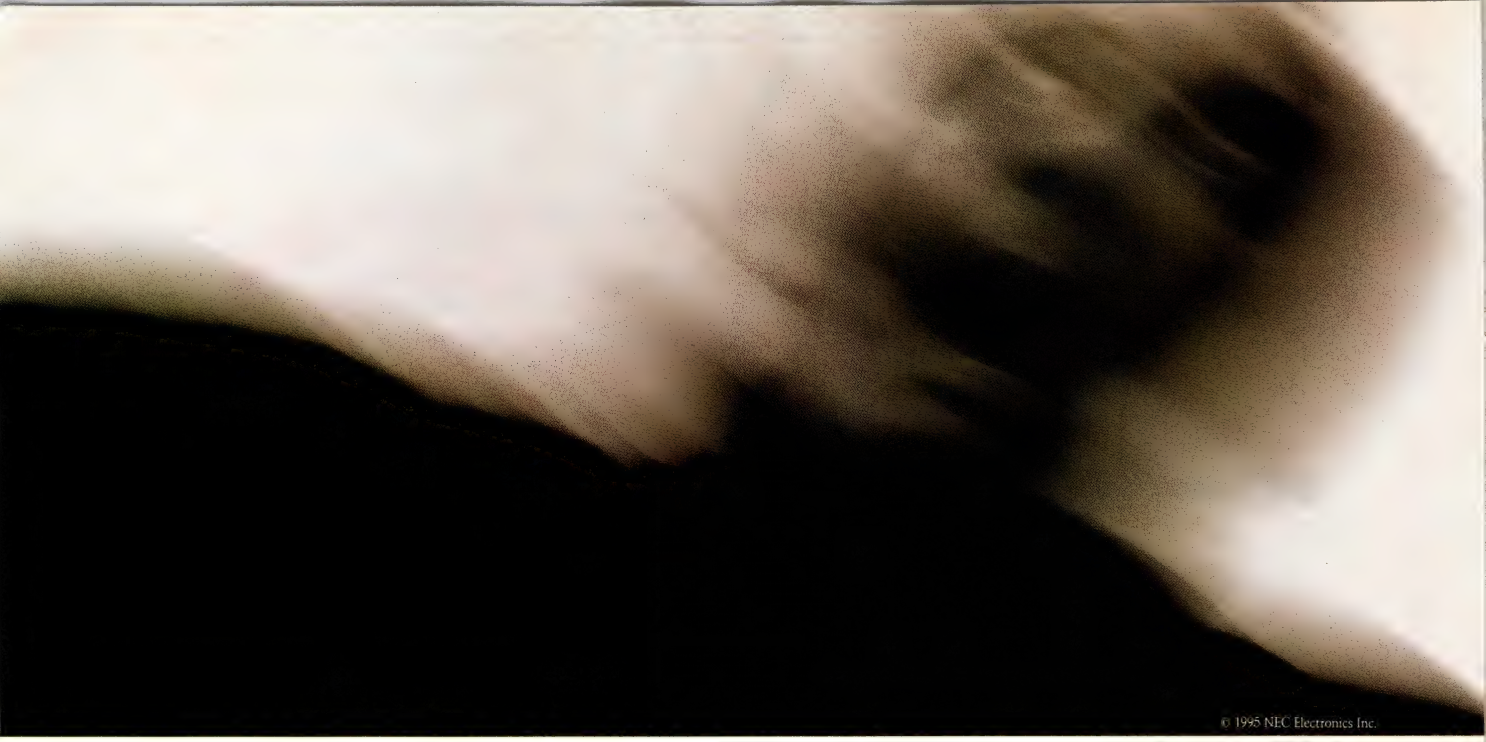

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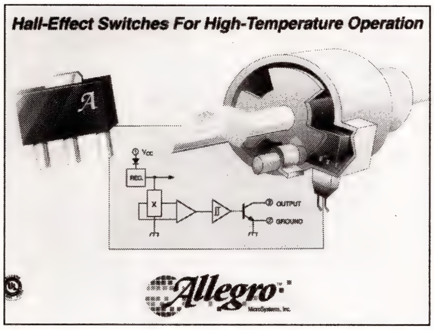
36-bit-wide bus logic for wide-bus applications. The Widebus+ SN74ABT-32xxx family of advanced bus logic has a 5-nsec propagation delay, provides –32- and +64-mA output drive, and is available in 80- or 100-pin plastic shrink QFPs. A bus-hold feature stores the last known state of the bus, avoiding the need for discrete pullup resistors. You can sue the transparent, bidirectional SN74ABT32245PZ data transceiver as four 9-bit, two 18-bit, or one 36-bit transceiver. $10.95 (1000). The 32543PZ 36-bit registered transceiver has two sets of D-type bidirectional latches for data storage. $12.10 (1000). Other family members include a 36-bit universal bus transceiver; a 16-bit, triport, universal-bus exchanger; and an 18-bit, triport, universal-bus exchanger. **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 361**



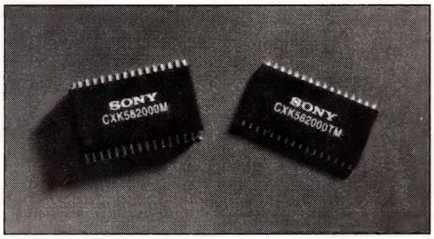
Hall-effect switches offer high-temperature operation. The A3121-A3123 and A3141-A3144 Hall-effect switches are available in temperature ranges of –40 to +150°C. The switches operate from 4.5 to 24V dc and have open-collector outputs that sink up to 25 mA. The versions offer operating sensitivities from 100 to 350 gauss and hysteresis levels of 55 to 105 gauss. From $1.04 (1000). **Allegro MicroSystems Inc**, Worcester, MA. (508) 853-5000. **Circle No. 362**

16- and 32-Mbit mask ROMs operate below 3V with 150-nsec access time. The mask ROMs operate from 2.7 to 3.6V supplies, dissipating 35 mA while operating and 30 μA in standby mode. The devices come in 44-pin SOP and 48-pin TSOP packages. The 16-Mbit LH53V16500 costs $20 (100), and the 32-Mbit LH53V32500 costs $30 (100). **Sharp Electronics Corp**, Camas, WA. (206) 834-2500. **Circle No. 363**

QAM digital-transmission receiver for cable TV increases channel capacity. The single-chip BCM3100 QAMLink, a 64/256-quadrature-amplitude-modulation (QAM) digital-transmission receiver, suits cable-TV applications. In the 256-QAM mode, it achieves 40-Mbps digital-transmission speeds. According to the company, the chip increases the channel capacity of coaxial cable by a factor of 10 to 25. The chip integrates QAM demodulation, Nyquist filtering, carrier and timing synchronization, and adaptive equalization. The IC comes in an 80-pin

PQFP and costs $50 (1000). **Broadcom Corp**, Los Angeles, CA. (310) 443-4490. **Circle No. 364**

DAA chip set provides 6-kV isolation for fax/modem cards. The K^2 data-access-arrangement (DAA) chip set connects to a telephone line tip and ring signals. The set includes an eight-pin SOIC, a 16-pin QSOP, and a 20-pin QSOP. The three chips are 1.4 mm high and mount inside fax/modems, including PCMCIA cards. The chips accommodate 300- to 28.8k-bps V.34 data rates and provide off-hook relay control, ring-indication output, internal two- to four-wire conversion, voice/data control, and caller ID. The chips operate from 3.3 or 5V and have a 30-mW active power consumption and a 10-mW standby power consumption. Protection circuitry meets FCC Part 68, DOC CS-03 European isolation standards, and UL 1459 requirements for hazardous voltage and leakage. $8.50 (10,000). **Krypton Isolation Inc**, Fremont, CA. (510) 713-9100. **Circle No. 365**



2-Mbit SRAM has 85-nsec access time and is pin compatible with 1-Mbit RAMs. The CXK58200 is a 256k×8-bit CMOS SRAM with an 8-μA standby current and a 4.8-μA data-retention current at 40°C. A version with an 85-nsec access time costs $40, and a 100-nsec version costs $30. **Sony Electronics Inc**, San Jose, CA. (800) 288-7669. **Circle No. 366**

Stackable 3-D flash-memory module provides up to 128 Mbits of high-density storage. Commercial flash-memory modules range from 16 ($213 (100)) to 128 Mbits ($1638 (100)). Military modules range from $261 (100) to $2019 (100). The stacking modules permit placing more memory per square inch of board space than with nonstacking memory. SRAM modules are also available. **DensePac Microsystems**, Garden Grove, CA. (714) 898-0007. **Circle No. 367**

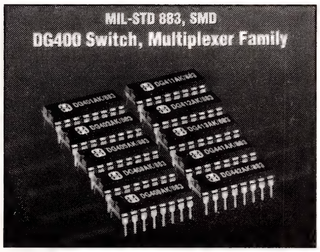
Multimedia reference design provides an MPEG-compliant add-in board for <$100 in volume. The reference design for PC add-in cards extends the multimedia capability of a PC to play full-resolution, -motion video and CD-stereo sound. The design uses TI's TMS320AV220 video-CD MPEG-1 decoder, TI's TMS320AV120 MPEG audio decoder, and AuraVision's VxP201 video-playback processor. The three ICs form the core of the full-motion, video-playback board, featuring an ISA bus interface, support for up to 1280×1024-pixel resolution, interpolated zoom, and full color control. The design kits include a suite of driver software licensed by AuraVision to complement the hardware design for Windows 3.x and DOS. The design kit includes an evaluation board, schematics, a parts list, pc-board layout, software, and documentation for $3000. **AuraVision**, Fremont, CA. (510) 252-6800. **Circle No. 368**

3.3V FPGAs suit portable-computing applications. Devices from the company's ACT1 and ACT3 family are available in 3.3V versions. The 1200-gate A10V10B and the 2000-gate A10V20B are from the ACT1 family. The ACT3 family includes devices with 1500 to 10,000 gates. The company is also offering new packaging options, including the 1-mm-thick VQFP package for FPGAs (field-programmable gate arrays) with up to 4000 gates. The TQFP is available for 4000- to 6000-gate devices and meets the specifications for Type II and Type III PCMCIA cards. The 10,000-gate part comes in a 313-lead ball-grid array. ACT1 devices start at $7 for the A10V10B, and ACT3 devices start at $17.70 (OEM) for the 1500-gate A14V15A. **Actel Corp**, Sunnyvale, CA. (408) 739-1010. **Circle No. 369**

4- and 16-Mbit DRAMs offer extended data output for 25-nsec page-cycle times. The 1M×4-bit HM514405C extended-data-output DRAM has a 1k/16-msec refresh; 60-, 70-, or 80-nsec row-address access times; and 25-, 30-, and 35-nsec row-address access times for a continuous burst of address retrieves. A device with the 60-nsec row-address access time and 25-nsec address-access cycle time costs $22 (1000). The 1M×16-bit HM5116165A DRAM has a 4k/64-msec refresh and costs $110 (1000) for the 60-nsec row-access and 25-nsec address-access cycle-time version.

Hitachi America Ltd, Semiconductor and IC division, Brisbane, CA. (800) 285-1601, ext 11. **Circle No. 370**

Low-power wireless prescalers for personal communication services. The PMB 2313 prescaler for mobile-radio devices up to 1.1 GHz suits battery-powered systems, such as cellular phones, cordless telephones, and wireless LANs. The low-power device operates from voltages as low as 2.7V and offers a standby mode. The PMB 2314 is for similar applications up to frequencies of 2.1 GHz and offers 2.7V operation. Each costs $2.61 (1000). **Siemens Components Inc, Integrated Circuits Division**, Cupertino, CA. (408) 777-4500.
Circle No. 371



Analog-switch family has MIL-STD-883 and standard-microcircuit-drawing (SMD) number classifications. The DG400 analog-switch family includes 10 devices that operate from –55 to +125°C. Prices range from $7.44 (100) to $18.29 (100). **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7290. **Circle No. 372**

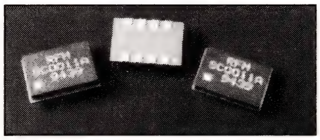
V.32bis modem chip set for Windows PCs costs $29. The HSM192DW controllerless modem chip set uses the system host CPU (386, 486, or Pentium) to perform modem microcontroller software functions, such as AT commands, data compression, and error correction. This approach eliminates the need for a modem controller chip, RAM, and ROM. The change saves board space, power consumption, and cost, according to the vendor. The chip set works with Microsoft's Windows architecture, the standard Windows communications driver, and virtually any communications or fax application for Windows. The chip set supports data rates and fax speeds up to 19.2k bps, the AT Command Set, V.42 and MNP4 error correction, and V.42bis and MNP5 data compression. The HSM192PW chip set supports the PCMCIA standard and costs $31 (100,000). **AT&T Microelectronics**, Allentown, PA. (800) 372-2447.
Circle No. 373

Arrays of MOSFET power transistors provide fast switching and eliminate voltage-level shifting. The Power+monolithic arrays have a 5V logic-level interface, eliminating the need for predrive voltage-shifting circuitry. The power-transistor arrays provide switching speeds to drive fractional horsepower motors in high-frequency applications. Arrays of three, four, or six power DMOS transistors are available. Typical on-resistance is 0.4Ω, and peak current is 3A/channel. Voltage rating is 60V. From $1.37 (1000). **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 374**

12-bit, 20M-sample/sec ADCs offer low distortion. The TTL-compatible AD9022 and the ECL-compatible AD9023 have a spurious-free dynamic range of 75 dB at 1 MHz and 74 dB at 9.6 MHz. The converters have an analog input bandwidth of 100 MHz, well beyond the Nyquist limit for the devices, suiting them to direct intermediate frequency to digital conversion or undersampling. The dynamic nonlinearity is <0.5 dB, and the S/N ratio is typically 65 dB. The devices provide a track-and-hold amplifier, a reference, and control logic and timing. Both parts require +5V and –5.2V. Typical power dissipation is 1.3W. Available in 28-pin ceramic DIP and surface-mount packages, they cost $140 (1000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1428.
Circle No. 375

Op amp offers high-voltage, 2A output-current capability. The OPA544 operates from ±10 to ±35V supplies and has a slew rate of 8 V/μsec. The device drives electromechanical devices, including motors, valves, and speakers. It also suits programmable power supplies and magnetic deflection-coil drivers. Other features include a 100-pA input-bias current, internal current limit, and internal thermal-shutdown protection when junction temperature reaches approximately 165°C. The device operates from –40 to +85°C. Housed in a five-pin TO-220 package, the device costs $6.95 (100). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111.
Circle No. 376

Addressable scan-port device extends boundary-scan testing to system level. The SN54/74ABT8996 addressable scan-port device permits the testing of boards in a system using IEEE 1149.1 boundary-scan chip- and board-level test patterns without reformatting. The device acts as a serially addressable switch that directly interfaces primary test-access-port (TAP) signals to secondary TAP signals. Instead of requiring each board in a system to have its own dedicated test-mode line on the backplane, the device lets up to 1021 boards share one multidrop test mode line. $6 (1000). **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500.
Circle No. 377



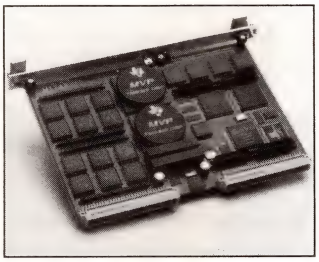
Surface-mount clocks offer 300- to 700-MHz frequency. The SC00xx family of digital clocks provides better power-supply noise immunity and less jitter than conventional ECL or PLL clocks, according to the maker. The differential sine-wave clocks feature a worst-case symmetry of 48 to 52%, a typical period jitter of 15 psec p-p, and a maximum jitter of 30 psec p-p. From $13.50 (1000). **RF Monolithics Inc**, Dallas, TX. (214) 233-2903. **Circle No. 378**

Hall-effect gear-tooth sensors operate down to zero speed. The A3046, A3056, and A3058 Hall-effect sensors are monolithic ICs that switch in response to differential magnetic fields that ferrous targets create. When you combine the devices with a back-biasing magnet, the sensors can provide a 50% duty cycle or switch on the leading or trailing edge, or both, of a passing gear tooth or slot. Each device contains two quadratic Hall-effect sensing elements, a voltage regulator, temperature-compensating circuitry, a low-level amplifier, a Schmitt trigger, and an open-collector output driver. The sensors operate over wide temperature ranges, making them suitable for industrial and automotive applications, such as antilock braking and ignition timing. From $1.94 (1000). **Allegro MicroSystems Inc**, Worcester, MA. (508) 853-5000.
Circle No. 379

Embedded development tools for the Motorola 68HC11, 68HC16, and 68000 family µCs. The Pentica MIME-600 emulator for 8-bit targets ($9984) and the MIME-700 emulator for 16-bit targets ($14,159) feature unlimited hardware breakpoints; a bus event triggering subsystem; a prefilterable trace buffer; and C source-level debugging. The Cosmic Software development tools are a Windows application, integrating a compiler, debugger, and programming utility. The software costs $2500 for the 68HC11, $3000 for the 68HC16, and $3400 for the 68000 family. **Pentica Systems Inc**, Bedford, MA. (617) 275-4419.
Circle No. 404

Ada 9x development system for embedded processors. Version 5.1 of the Ada development system provides significantly improved tools over previous releases. A simple command-line switch lets system users begin working with the features of Ada 9x without disrupting Ada 83 code. The company's Ada cross-compilation development systems work with TMS320C3x, TMS320C40, i960, 68xxx, and MIL-STD-1750A processors. The devices are hosted on Sun SPARC and DEC VAX/VMS workstations. From $20,000. **Tartan Inc**, Monroeville, PA. (412) 856-3600. **Circle No. 405**

Type II PCMCIA card provides sound and SCSI-2 interface. The Sound/SCSI-2 card enables the use of CD-ROM-based multimedia programs that include sound in portable PCs equipped with a single PCMCIA slot. The card features hot insertion and removal, 16-bit transfer at 10 Mbytes/sec over SCSI-2, and 16-bit sound with a sample rates up to 44.1 kHz. $369. **Cardwell International Corp**, Folsom, CA. (916) 985-1880.
Circle No. 406



Single-slot VME board uses dual TMS320C80 multimedia video processors. The MZ 4700 is a DSP board for high-end imaging and audio applications, such as document storage and retrieval, virtual reality, video conferencing, and intense graphic manipulations. You can configure the board with one or two 40-MHz multimedia video processors (MVPs). With two MVPs, the board is capable of four billion operations per second (BOPS). The board has a master/slave VME64 interface for fast data transfers over the VMEbus. Internal communication channels are capable of 320 Mbytes/sec data transfer rates. The board costs $21,995 (OEM qty) and will be available in the second quarter. **Mizar Inc**, Carrollton, TX. (214) 277-4600.
Circle No. 407

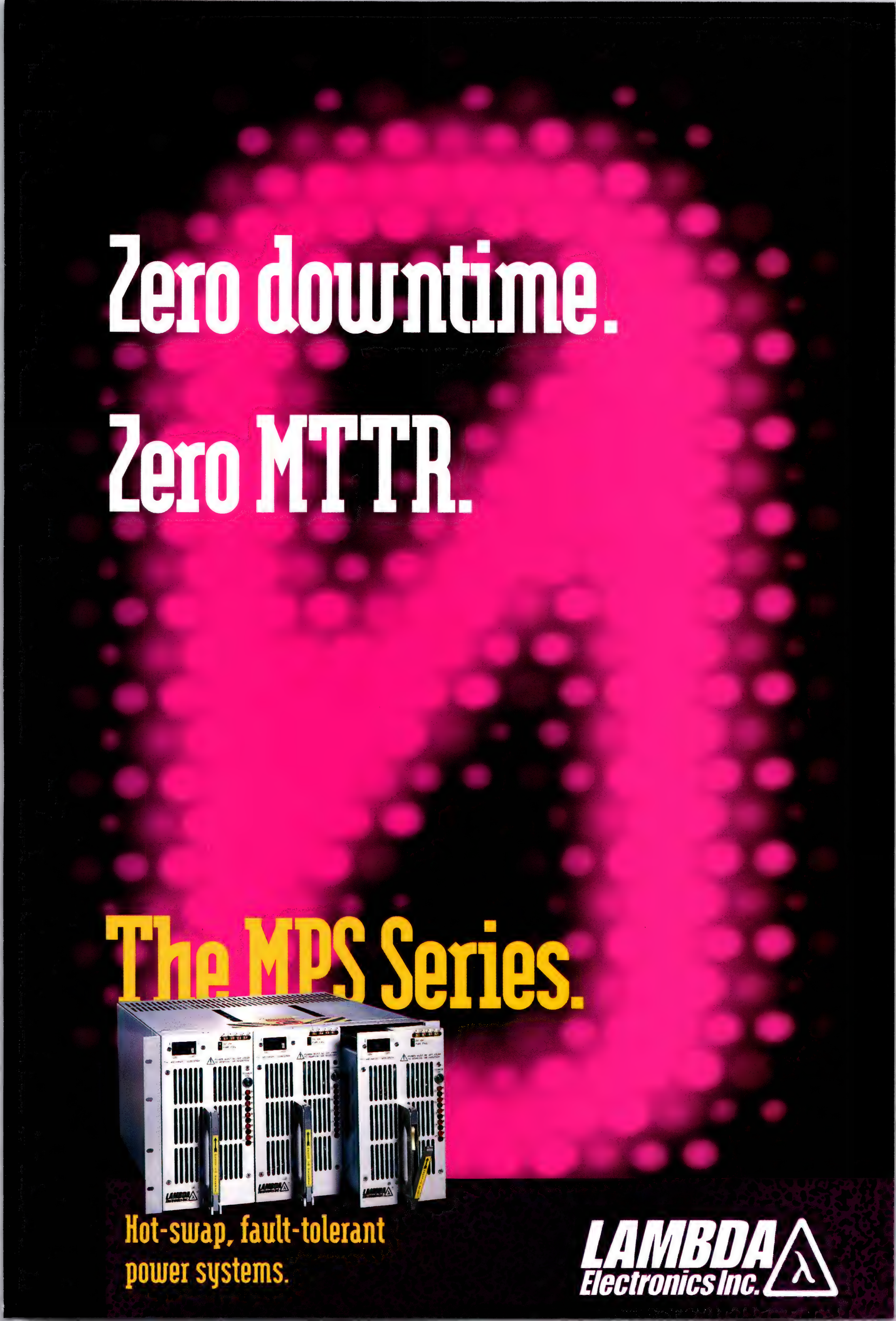
DSP-based voice-processing algorithms available in open architecture. VP Open provides algorithms used in voice conferencing, voice multiplexing, and voice-messaging systems. Specific algorithms handle voice compression, DTMF detection and removal, dial-pulse detection, echo cancellation, a speech detector, call-progress tone detection, and time-scale modification of speech to preserve speaker voice quality and speech intelligibility. The VP open development package costs $4950. Algorithm modules are available as individual porting packages and cost from $1950 to $9950. **D2 Technologies**, Santa Barbara, CA. (805) 564-3424.
Circle No. 408

Windows-based software tool helps program embedded processors and controllers. ApBuilder is a free interactive tool that includes support for the 386 EX processor and the newest versions of the company's µCs. The software lets you select the configuration of the desired peripherals with a mouse, and the software generates the complete initialization code for the device in Assembler or C. **Intel Corp**, Santa, Clara, CA. (800) 486-8118 ext 226.
Circle No. 409

APFDDI for VMEbus provides redundant operation. The 100-Mbps PT-VME60X, fiber-distributed-data interface (FDDI) node adapter, the hot-swappable PT-VME61X FDDI concentrator, and the ACC60X FDDI backplane adapter provide a stand-alone, alternate-path FDDI (APFDDI) node. The node occupies two slots in a standard VME card cage and complies with ANSI, survivable, adaptable, fiber-optic embedded-network (SAFENET), Mil 2204A, and HDBK 818A standards. $9815. **Performance Computer**, Rochester, NY. (716) 256-0200. **Circle No. 410**

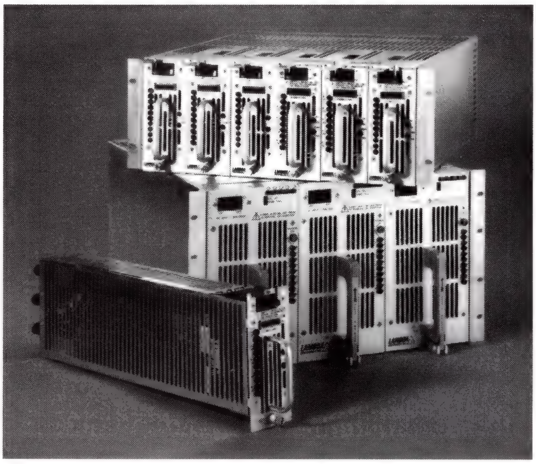
Tool automates the development and deployment of real-time, data-driven graphical interfaces. The VAPS suite provides a range of tools from an entry-level prototyping tool to an advanced environment for applications running on multiple platforms. VAPS/Prototyper ($9500) is an entry-level tool for human-factor specialists and designers who need only to prototype real-time interactive graphical applications. VAPS/Designer ($16,500) suits advanced real-time interactive graphical prototypes. VAPS/Developer ($34,500) generates C code for users going beyond the prototyping phase. VAPS/Rehost ($41,500) is a development tool providing prototyping through deployment on multiple target platforms. **Virtual Prototypes Inc**, Montreal, Canada. (514) 341-3874.
Circle No. 411

In-circuit emulator for AM29200 and AM29240 RISC µC families. The SYS29K-Panther supports the µC in all modes of operation at the full-rated speed. A real-time profiler collects information about target system behavior. The profiler records processor activity on every clock cycle, even if it is being executed from cache. The emulator has overlay memory options of 256 kbytes, 1 Mbyte, or 4 Mbytes. The system accommodates dynamic bus sizing, burst-mode operation, and bus widths of 8-, 16-, and 32-bits. $24,495. **Embedded Performance Inc**, Milpitas, CA. (408) 434-2210.
Circle No. 412



Zero downtime.
Zero MTTR.
The MPS Series.
Hot-swap, fault-tolerant power systems.
LAMBDA Electronics Inc.

Lambda's MPS Series



Hot-swap, fault-tolerant power systems.

Lambda's MPS Series Modular Power Systems are easily configured to meet any custom requirement – from fault-tolerant N+1 redundant, to high power and scaleable configurations. The MPS Series consists of single and multiple output power supplies from 340W to 1800W, with up to five outputs per module, with or without a system enclosure.

With its low MTTR, an MPS system is ideal for applications such as communications and industrial controls, which can't tolerate disruption of DC power.

Designing your complete MPS Modular Power System is as easy as calling 1-800-LAMBDA-4. You specify the requirements – we'll do all the work.

Redundant, Fault-Tolerant Operation	Ensures zero downtime and fail-safe operation for critical power applications.
Hot-Swap, Live Insertion/ Extraction While the System is "On"	Reduces MTTR (Mean Time To Repair/Service) to zero without system down time. Cam action handle ensures the power supply is off when removed.
Broad Range of Single and Multiple Outputs	This complete selection shortens design cycle time and enables the user to specify a system that meets their exact requirements.
System Interface and Indicator Signals	AC Fail, Output Inhibit and Output Power Fail Signals coupled with appropriate visual indicators ensure ease of use and ease of system integration.
Fail Safe Design	Automatic current share disconnect prevents corruption of surviving supplies upon a single point failure.
Scaleable Power Building Blocks	Provides the ability for increased power and field expandability.
Turn-key System Solution	Complete building block approach featuring integral keyed power and signal interface connectors, backplane, and enclosure.
Meets Worldwide EMI Requirements	Conducted EMI conforms to FCC 20780 and VDE 0871 Curve A to meet worldwide requirements.
Power Factor Correction and Harmonic Distortion	Active power factor correction circuitry ensures compliance to IEC 555-2 while improving input power quality, line regulation, AC noise immunity and holdup time.
Worldwide Safety Agency Approvals	Safety agency approvals to UL 1950, CSA, and EN 60950 ensures compliance throughout the world.
3 Year Guarantee	Lambda's MPS Series is backed by a three year guarantee that includes labor as well as parts.

MPS Series Single Output

MAX POWER	OUTPUT 1	MODEL
340	48V@6.7A	PS-4
900	2-4V@200A	PS-31S-1KW
900	4-6V@ 190A	PS-31S-1KW
900	7-12V@ 84A	PS-31S-1KW
900	12-28V@36A	PS-31S-1KW
900	28-56V@18A	PS-31S-1KW
1350	7-12V@125A	PS-31S-1.5KW
1350	12-28V@54A	PS-31S-1.5KW
1350	28-56V@27A	PS-31S-1.5KW
1800	7-12V@167A	PS-31S-2KW
1800	12-28V@72A	PS-31S-2KW
1800	28-56V@36A	PS-31S-2KW
1800	48V@38A	PS-31S-2KW

MPS Series Dual Output

MAX POWER	OUTPUT 1	OUTPUT 2	MODEL
1080	5V@190A	2-4V@20A	PS-31M-1.5KW

MPS Series Triple Output

MAX POWER	OUTPUT 1	OUTPUT 2	OUTPUT 3	MODEL
340	2-6V@54A	5-15V@11A	5-15V@11A	PS-4
900	5V@150A	5-15V@20A	5-15V@20A	PS-31M-1KW
900	5V@150A	5-24V@10A	5-24V@10A	PS-31M-1KW
1350	5V@190A	5-15V@20A	5-15V@20A	PS-31M-1.5KW
1350	5V@190A	5-24V@10A	5-24V@10A	PS-31M-1.5KW

MPS Series Quad Output

MAX POWER	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	MODEL
340	2-6V@54A	5-15V@11A	5-15V@11A	5-15V@11A	PS-4
340	2-6V@54A	5-15V@11A	5-15V@11A	12-28V@6A	PS-4
340	12-28V@13A	5-15V@11A	5-15V@11A	12-28V@6A	PS-4
500	2-6V@54A	5-15V@11A	5-15V@11A	5-15V@11A	PS-4
900	5V@150A	5-15V@20A	5-15V@20A	5-24V@10A	PS-31M-1KW
1350	5V@190A	5-15V@20A	5-15V@20A	5-24V@10A	PS-31M-1.5KW

MPS Series Pent Output

MAX POWER	OUTPUT 1	OUTPUTT 2	OUTPUT 3	OUTPUT 4	OUTPUT 5	MODEL
500	2-6V@54A	2-6V@22A	5-15V@11A	5-15V@11A	5-15V@11A	PS-4
500	12-28V@13A	5-15V@11A	5-15V@11A	5-15V@11A	12-28V@6A	PS-4
900	5V@150A	5-15V@20A	5-15V@20A	5-24V@10A	5-24V@10A	PS-31M-1KW
1350	5V@190A	5-15V@20A	5-15V@20A	5-24V@10A	5-24V@10A	PS-31M-1.5KW

Power Enclosures 19" Rack Mountable

MODEL	DIMENSIONS	CAPACITY
PE-4-3	7"H x 10.5"W x 19"D	Up to three PS-4 Series Plug-in Power Supplies
PE-4-6	7"H x 19"W x 19"D	Up to six PS-4 Series Plug-in Power Supplies
PE-31-3	10.5"H x 19"W x 20"D	Up to three PS-31 Series Plug-in Power Supplies

Accessories Mating Connectors

Mating connector kits are available directly from Lambda, consult the factory.

Blanking Plates Covers One Slot

PART #	
BPK-4	Fits PE-4 enclosures
BPK-31	Fits PE-31 enclosures

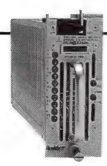
How to Configure Your Own Modular Power System

1. List Your Requirements

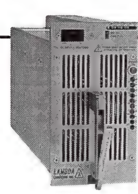
	VOLTS		AMPS PER SUPPLY		OUTPUT POWER	AMPS NEEDED FOR TOTAL SYSTEM LOAD
Output #1:	______	x	______	=	______	______
Output #2:	______	x	______	=	______	______
Output #3:	______	x	______	=	______	______
Output #4:	______	x	______	=	______	______
Output #5:	______	x	______	=	______	______

NOTE: Outputs include isolation diodes and automatic current sharing.

2. Select Your Plug-In Power Supply



PS-4 Series	TOTAL OUTPUT POWER PER SUPPLY	INPUT VOLTAGE (Check one) AC w/PFC	DC (48 VDC)
7"H x 2.8"W x 19"D	340 Watts	______	______
	500 Watts	______	NA



PS-31 Series	TOTAL OUTPUT POWER PER SUPPLY	INPUT VOLTAGE (Check one) AC w/PFC	DC (48 VDC)
10.5"H x 5.6"W x 20"D	900 Watts	______	NA
	1350 Watts	______	NA
	1800 Watts	______	NA

3. Call 1-800-LAMBDA-4 from 8:00 am to 8:00 pm (East Coast Time)

with your requirements and we'll design your complete power system.

The Modular Power System (MPS) consists typically of a 19" rack mountable Power Enclosure (PE) which holds a number of Plug-In Supplies (PS). The Plug-In Supplies come in various sizes and power ranges to match your requirements.

Here are the simple steps to follow to configure your own MPS.

1. List your output requirements for each Plug-In Supply and for your total system load (if you are paralleling two or more supplies for redundancy or higher currents). Multiply your volts times the amps for each output to determine the output power.

2. Select the Plug-In Supply (PS) from the selector guides which best match your power requirements. Although many standard output voltage combinations are listed in the selector guides, others are readily available – contact the factory for details. For a convenient means of mounting the Plug-In Supplies, refer to the Power Enclosure (PE) information contained in this brochure.

Plug-In Supply (PS) Selector Guides

The selector guides are partial listings of standard models. Many other models are available to meet your needs; simply contact the factory at 1-800-LAMBDA-4 for model numbers. The voltage ranges listed in the guides are selection ranges, not adjustment ranges. All outputs are factory set to your exact specifications.

MPS Series Specifications

AC Input

line . . . . 90 - 264VAC, 47- 63Hz on PS-4 and PS-31-1K Series.
180 - 264VAC, 47 - 63Hz on PS-31-1.5K, PS-31-2K Series.
36 - 72VDC input available on PS-4 Series. Consult Factory.

In-rush Current

20A PK on PS-4.
80A PK on PS-31.

Efficiency

75% Typical.

EMI

Conducted EMI conforms to FCC20780, Part 15, Subpart J, Class A and VDE 0871 Class A.

Input Harmonic Current

Meets IEC 555-2 harmonic distortion.

Circuit Breaker

All power supply modules are provided with a front panel mounted input circuit breaker.

DC Output

Voltage ranges are shown in tables.

Regulated Voltage

line regulation . . . . 0.2% of rated output voltage.
load regulation . . . . . . 0.8% max of rated output voltage.
ripple and noise . . . . . 1% pk-pk max.
temperature coefficient . . . . 0.02%/°C.

Thermal Protection

The power supply will automatically shut down in the event of an overtemperature condition. To reset, recycle input power.

Overcurrent Protection

Factory set at 110% to 120% of current rating. Automatic recovery upon removal of overload condition.

Overvoltage Protection

When the individual output exceeds the overvoltage set point, the output will shut down. Trip points are factory set within 120% to 130% of nominal output voltage. Trip point for 2V outputs is factory set at 3.0V to 3.5V. An OV condition on channel 1 of PS-31 will shut down the entire power supply.

Preload

Channel 1 on PS-31 requires a minimum load of 10% for the 5V output, 20% for other voltages. 0.5A minimum load required when auxilliary outputs are adjusted to greater than 18V.

For proper operation of current share and DC OK indicators, paralleled auxilliary outputs require a minimum load of 10% for outputs less than 24V and 20% for outputs greater than 24V.

Hold-up Time

At full load and nominal AC line, outputs will remain within regulation limits for a minimum of 16msec after loss of AC power.

Remote Sensing

Sense lines will compensate for a 0.5 VDC total cable drop. Internal circuitry protects the load if sense lines are opened.

Current Sharing

Equivalent outputs with the current share option may be paralleled and will current share within ±5% of total load.

Remote On/Off

PS-4: A TTL high will disable the entire power supply.
PS-31: A TTL low signal referenced to sense will disable the main output. Individual TTL high signals inhibit the auxilliary outputs.

Input Power Indicator

The green indicator is on when input power is present.

Remote Monitoring Signals

Input power fail, DC output fail signals and DC OK/power fail indicators are standard.

Test Points

Test points are provided on the front panel for each output.

Isolation Ratings

Input to Output:	2200V RMS
Input to Chassis:	2200V RMS
Output to Chassis:	100V RMS

Cooling

All power supply modules are forced air cooled via internal fan.

Operating Temperature Range

100% rated power from 0 to +50°C for PS-31. 0 to +40°C for PS-4.

Storage Temperature Range

–40°C to + 85°C.

DC Output Controls

Outputs are factory set to user specified voltages and should not be adjusted, since it will interact with factory settings for OVP, current share and power fail circuits.

Shock and Vibration (non-operating)

Shock: 15G half sine, 11msec, 3 axes, 3 impulses
Vibration: 0.01G2/Hz from 20Hz to 500Hz, 1 octave per minute, 10 minute dwells at each resonant frequency (up to 4) on each axis, 1 sweep per axis, 3 sweeps total.

Physical Data

Model	Weight (Lbs.)	Dimensions (inches)
PS-4 Power Supply Modules	14 lbs.	19.29 x 2.73 x 6.91
PS-31 Power Supply Modules	32 lbs.	20.13 x 5.53 x 10.41
PE-4-3 Power Enclosure	12 lbs.	19.00 x 10.52 x 6.97
PS-4-6 Power Enclosure	17 lbs.	19.00 x 19.00 x 6.97
PE-31 Power Enclosure	27 lbs.	20.00 x 19.00 x 10.47

Safety Agency Approvals

UL1950, CSA22.2 234 M90 for PS-31. CSA1402C for PS-4, EN60950 approvals have been received on some models and may be pending on others. Consult the factory for specifics.

Guarantee

Three year guarantee includes labor as well as parts. Guarantee applies to operation within published specifications at the end of three years.

Real-Time Solutions for PowerPC.

SHIPPING TODAY

Microware's OS-9 Real-Time Operating System puts real-time for the PowerPC in your hands today. OS-9 for PowerPC is available for the 4XX, 5XX and 6XX processor families with off-the-shelf I/O to support virtually any demanding real-time application. Plus, OS-9 for PowerPC supports systems of any size — from small ROM-based devices to large-scale networked products.

TIGHTLY INTEGRATED TOOLS

To accelerate your project, Microware puts easy-to-use development tools at your fingertips. FasTrak is Microware's development environment built around Ultra C, our ANSI C compiler. Ultra C is the first ANSI C compiler to bring true interprocedural and global optimization to the PowerPC architecture. The tight integration of OS-9 and development tools boosts your productivity and reduces your time-to-market.

PROVEN QUALITY

OS-9 for PowerPC expands upon Microware's proven success in the system software industry. In over 4,500 products, designers have relied on Microware's quality solutions for their demanding applications. Microware's total commitment to this quality and reliability is reflected in our recent ISO 9001 certification by Underwriters Laboratories (UL), the first such certification in the system software industry.

Learn how OS-9 for PowerPC can handle your real-time design challenges — today. Call Microware toll-free at 1-800-475-9000 for a free copy of the *OS-9 for PowerPC White Paper.*

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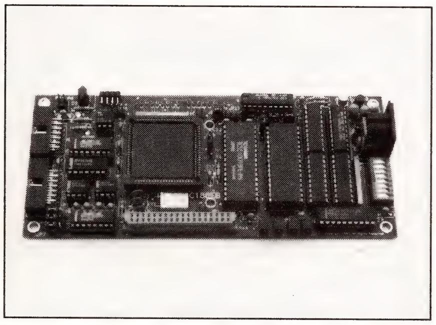
1900 N.W. 114TH ST. DES MOINES, IA 50325-7077 1-800-475-9000 OR (515) 224-1929 FAX: (515) 224-1352 INTERNET: info@microware.com

CIRCLE NO. 111

Design tool provides state chart synthesis, analysis, and code generation. StateCAD 2.0 is a Windows-based design tool for specifying control flow, parallel processes, and message transfer. The tool provides a means of resolving real-time embedded and DSP problems using prioritized control flow and concurrent processes. Optimizations include state enumeration, compiler-specific data types, graphical-message specification, and event scheduling. The tool produces ANSI-C code and costs $495. **Visual Software Solutions**, Coral Springs, FL. (305) 423-8448. **Circle No. 413**



Small, low-cost, 16-bit, single-board computer needs no bus. The 3×6.7-in. MICRO-C188EB board lets you develop custom products without a complex bus. The 20-MHz 80C188EB CPU works with up to 512 kbytes of SRAM and 512 kbytes of EPROM or flash EPROM. Onboard functions include an interrupt controller, three 16-bit counter/timers, two RS-232C/422/485 ports, a watchdog timer, power-failure detection, and two iSBX expansion ports. Many vendors offer iSBX modules for the board. $225 (low volumes). **RLC Enterprises Inc**, Atascadero, CA. (805) 466-9717. **Circle No. 414**

Development tool uses dual-ported memory architecture to monitor and modify target memory. UniROM provides access to target memory without wait states, arbitration, monitor programs, or other intrusive mechanisms that alter system performance. UniROM plugs into the target's memory socket instead of the CPU, making it compatible with any CPU type, speed, and package style. The tool emulates EPROM, flash, SRAM, or EEPROM as large as 32 Mbits and at access speeds as fast as 35 nsec. Advanced options include complex triggers, trace, and hardware breakpoints. 8- and 16-bit versions start at $495. **Techtools**, Garland, TX. (214) 272-9392. **Circle No. 415**

Debugger for multitasking RTOS. CMXBug debugs the company's CMX-RTX real-time operating system (RTOS). The RTOS lets you control tasks, events, messages, resources, cyclic timers, queues, fixed-memory blocks, and UARTs. The RTOS and debugger support various µPs; prices start at $875. **CMX Co**, Framingham, MA. (508) 872-7675. **Circle No. 416**

Object-oriented development environment now generates Smalltalk and Ada code in addition to C++. Software through Pictures for Object Modeling Technique (StP/OMT)

version 2.0, an object-oriented development environment, suits analysis, design, and code-generation applications. The new version provides incremental source-code generation for the Ada-83 language and support for 2167A documentation requirements. Jacobean Use Cases help model business processes. The tool set runs on Sun and HP workstations and costs $12,000. **Interactive Development Environments**, San Francisco, CA. (415) 543-0900. **Circle No. 417**

RFID-reader design kit. The Minireader radio-frequency-identification (RFID) kit lets you read transponder-equipped devices from a distance of several inches. The kit demonstrates all functions, except writing data to the transponder. It comprises a reader, which connects to a PC via an RS-232C interface; software; and six types of transponders. $200. **Deister Electronics USA Inc**, Manassas, VA. (703) 368-2739. **Circle No. 418**

Emulator upgrade for SYS29K-LYNX and SYS29K-PUMA ICEs accommodates the Am29040. The MINI-MANX emulator upgrade supports the Am29040 μP at clock speeds up to 25 MHz and is directly compatible with the 145-pin PGA ceramic package. The tool provides 2k words of trace memory with unlimited software breakpoints and up to 50 hardware breakpoints. A real-time profiler option provides information about target-system behavior. The upgrade for the SYS29K-PUMA in-circuit emulator (ICE) costs $2500, and the upgrade for the SYS29K-LYNX ICE costs $8000. **Embedded Performance Inc**, Milpitas, CA. (408) 434-2210. **Circle No. 419**

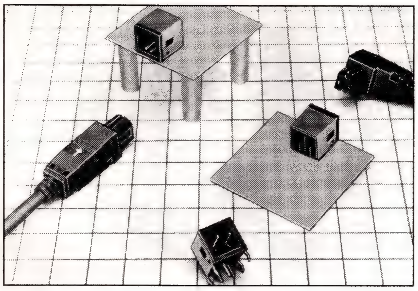
DSP development board for ISA bus provides dual-access memory. The Maestro 2100S is based on a 33- or 40-MHz TMS320C30 DSP and provides up to 8 Mbytes of zero wait state SRAM. 2 Mbytes of the SRAM may be shared with the PC/AT in a dual-access memory scheme. The company offers a prototyping daughterboard, including a fully labeled wire-wrap area. From $1950 with 1 Mbyte of memory. **Wintriss Engineering Corp**, San Diego, CA. (619) 550-7300. **Circle No. 420**

80C51-based single-board computer costs $49. The 1.625×2.25-in. Little Byte-51 operates at a clock speed of 12 MHz and has a 4-kbyte EEPROM for program storage. A DS1232 generates a power-on reset signal and provides an optional watchdog timer. Two 20-pin headers provide access to all CPU lines. A 20-MHz version costs $69. The device allows in-system programming using the company's PB-51/11 programming board ($99). **Allen Systems**, Columbus, OH. (614) 488-7122. **Circle No. 421**

80C32-based digital controller provides 12 digital I/O lines. The Xplor-32c provides a processor, 8 kbytes of EEPROM, a serial port, and a 5V regulator in a 5×2.5×1-in. protective enclosure. A Basic interpreter occupies the lower half of the block-protectable EEPROM, leaving the upper half available for Basic programs, data, and assembly-language programs. The controller costs $89.95. A starter package, including the controller, a user's manual, a PC serial-interface cable, a 9V power supply, and an application disk, costs $129.95. **Blue Earth Research**, Mankato, MN. (507) 387-4001. **Circle No. 422**

Write, edit, organize, and navigate through C and C++ source code with a GUI. The Object Master for Windows graphical user interface (GUI) joins the company's previous Macintosh tools, making it useful for cross-platform developers working on PC and Macintosh systems. The tool integrates with all major compilation systems, including Microsoft Visual C++, Symantec C++, Borland C/C++, and DOS compilers. The tool can trigger compilation and receive compilation errors without switching to the compiler environment. $249. **ACI US Inc**, Cupertino, CA. (408) 252-4444. **Circle No. 423**

COMPACT 3-POLE CONNECTOR FOR AC ADAPTER

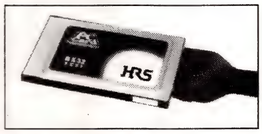


The RP34 is a compact, lightweight, 3-pole plastic connector specially designed for the AC adapter interface on notebook-type personal computers. Hirose's RP34 makes a plug available in either straight or right-angle type, the latter with a low-insertion profile. Ideal for office automation equipment, audio and small electronics products, the compact receptacle has a 10mm-square mating surface and 11.3mm depth. Hirose's snap lock permits easy insertion and disconnection and a D-shape mating section prevents mis-insertion. Assembly is easily made through a snap-fit assembly method for the plug, eliminating the use of screws.

For further information, contact **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958 or FAX (805) 522-3217.

CIRCLE NO. 26

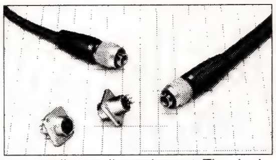
SCSI SHIELDED I/O CARD INTERFACE CONNECTORS



Hirose has introduced the NX 32, a 32-position SCSI shielded I/O card interface connector for use with PCMCIA and JEIDA PC cards. The NX series, available with frames and covers for secure latching, offers a super-low profile and a mounting height of only 2.9mm. NX series connectors have spacing of 0.8mm between contacts and are equipped with an inner lock. Joining NX series connectors available in 9-, 15-, and 25- positions, the NX 32 also meets PCMCIA I/O requirements for 1000 mating cycles. Ideal for either LAN or FAX/modem applications, they will fit Type I and Type II I/O cards (in accordance with both the JEIDA standard Ver. 4.1 and PCMCIA 2.0 standard). Hirose connectors are designed to include ESD and EMI protection.
For further information, contact **Hirose Electric (U.S.A.)**, 2688 Westhills Court, Simi Valley, CA 93065 (805) 522-7958 or fax (805) 522-3217.

CIRCLE NO. 28

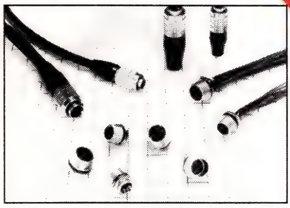
MINIATURE PUSH-PULL CONNECTORS FOR A/V USE



Hirose is offering the MXR series of miniature, lightweight, push-pull connectors with a ground function. These 3 and 8 contact MXR-type connectors are especially suitable for VTR camera and interfaces as well as audio equipment. The single-action push-pull lock function provides quick connections and disconnections as well as high density mounting. A "click" sound verifies that a secure engagement has been made. Tightening of the cable tube around the three conductors, without special tools, permits the cable to be clamped for improved workability.
For further information, contact the sales department, **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958 or fax (805) 522-3217.

CIRCLE NO. 29

WORLD'S SMALLEST ROUND, MULTI-CONTACT CONNECTORS ... ideal for outdoor use



Hirose is now providing the HR25 series of subminiature, round, multi-contact connectors. Ideal for use with miniature and high-density designs, the HR25 series offers a maximum of 20 contacts which have been condensed into an outside diameter of 12.5mm and a maximum of eight contacts into 10.5mm to achieve the world's smallest, high-density screw lock connectors. Available in a range of 4, 6, 8, 12, 16 or 20 contacts, the HR25 series is ideal for a wide range of applications, including CCD cameras, measuring instruments, sensors and interfaces for mobile radios.
For more information, contact the sales department, **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958 or fax (805) 522-3217.

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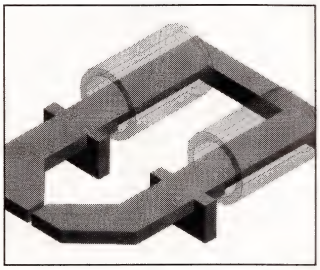
CIRCLE NO. 107

RF-filter design and analysis tool. Filter Designer Plus helps you design 14 of the most commonly used RF filters, including Butterworth, Chebychev, and elliptic. The tool also performs general filter-circuit analysis. Monte Carlo and yield analysis help you evaluate the effects of component tolerances on performance in your manufacturing process. The menu-driven tool with graphical user interface runs on PCs and costs $59.95. **TSV Engineering**, Raleigh, NC. (919) 846-2140.
Circle No. 391

Behavioral-synthesis tool simplifies the creation of finite state machines. The Parthenon behavioral-synthesis system uses a C- like language, called Structured Function description Language (SFL). SFL lets you work at a higher level of abstraction than other logic synthesis languages, such as VHDL. The language lets you create finite state machines that describe a system's behavior without regard to physical links, clocking, target technology, or physical implementation. According to the company, users have reported an 80 to 90% reduction in design time compar-ed with conventional logic-synthesis tools. $75,000 per license. **Harmonix Corp**, Woburn, MA. (617) 935-8335.
Circle No. 392

Network-management tool for voice and data networks. Cable System Manager 2.0 describes your company's cabling on computer with color maps, floorplans, pictures of all the wiring equipment, patch panels, cross-connect cables, hubs, outlets, and terminal equipment. Clicking on any connection brings up the entire data path with all its connect-points. The tool automatically validates the cabling architecture by checking the continuity of the data paths and the type of network and application for every wire. The device calculates statistics on the load of the system or any of its branches. The Windows-based tool starts at $2990. **Apsylog Inc**, Palo Alto, CA. (415) 812-7700.
Circle No. 393



Electromagnetic analysis tool solves Maxwell's equations for 2- and 3-D designs. MSC/EMAS electromagnetic-predictive tool solves Maxwell's equations in the static, frequency, and time domain. The software is designed for specific applications, including electrical apparatus for devices ranging from large power transformers to micro-motors; EMC (electromagnetic compatibility) and crosstalk, including radiation effects, shielding, and absorption properties of 2- and 3-D devices; RF and microwave designs, including waveguides, cavities, resonators, and connectors; and antennas, including wires, apertures, patches, and reflectors. The software leases for $1000/month. **MacNeal-Schwendler Corp**, Los Angeles, CA. (213) 258-9111. **Circle No. 394**

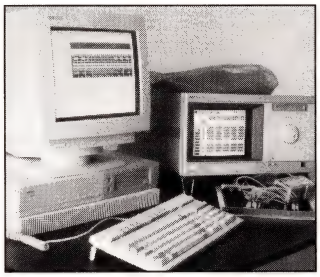
Graphical state machine and Petri-Net design tool generate Visual Basic code. BetterState is a diagrammatic programming tool for specifying the behavioral logic and sequencing behind a Visual Basic front-end design. Using extended state diagrams or Petri Nets, you draw the behavior sequencing you want, and the tool automatically generates the visual Basic code. The tool provides debug utilities to help you test the state transitions. BetterState Pro includes visual Basic, C, C++, VHDL, and Verilog code generation for $495. A stand-alone product for Visual Basic costs $295. **R-Active**, Cupertino, CA. (408) 252-2808.
Circle No. 395

RC-analysis and -reduction tool promotes fast simulation of networks in submicron designs. ΨCrunch compresses about 150,000 RC elements per minute to help achieve fast simulation of large submicron circuits while maintaining accurate models of the RC characteristics. The company claims the tool can reduce RC data by 50 to 80%, yet maintain accuracy of the original circuits to 1%. From $20,000 to $50,000. **Integrated Silicon Systems Inc**, Research Triangle Park, NC. (919) 361-5814.
Circle No. 396

Schematic capture and pc-board layout tool adds autoplacement. The HiWire II placement optimizer uses two algorithms. Quadratic programming gets the components in the right neighborhood, and simulated evolution further refines the placement. You can interrupt the tool while it is running to manually place components and change orientations. HiWire II with the placement optimizer and autorouter costs $1995. The standard HiWire product costs $995. **Wintek Corp**, Lafayette, IN. (317) 448-1903. **Circle No. 397**

MCM-layout tool adds automatic routing of pin escapes. Finesse MCM version 5.1 works with single-chip packages, ball-grid arrays, and MCMs (multichip modules). The release includes automatic filleting, automatic routing of pin escapes, and 3-D routing of complex via structures. A shape-based, push/shove router is optional. The tool costs $10,500 and is fully integrated with EDA navigator, which starts at $30,000. **Harris Electronic Design Automation Inc**, Fishers, NY. (716) 924-9303.
Circle No. 398

High-frequency design software adds coplanar waveguide library. The HP E4635A ArguMens Coplanar Waveguide Library complements the company's series IV high-frequency design-software-suite transmission-line models by adding 12 coplanar waveguide elements. $12,000. **HP-EEsof**, Westlake Village, CA. (818) 879-6200.
Circle No. 399



Software links HP logic analyzers and EDA tools. Wave-Link 16500 is a graphical environment that links the Hewlett-Packard HP-16500 logic analyzer and pattern-generator mainframe with EDA tools for verifying hardware against design test vectors. The system lets you use the same stimulus used in design for checking the hardware. The software costs $10,400. **Diagonal Systems Inc**, Palo Alto, CA. (415) 595-2266.
Circle No. 400

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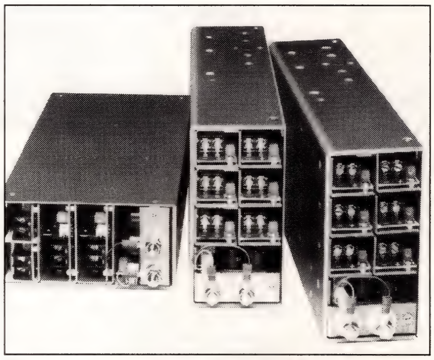
Rack-mounted, redundant-output power supplies provide up to 1200W. The redundant-output power supplies comprise a 19-in. rack-mounting assembly containing two modular power supplies. The supplies are interconnected to provide rated output to the load without interruption, even if one power supply fails. You can safely remove or replace the defective supply without tools while the system remains in operation. The supplies include overvoltage protection and a voltage-monitor circuit, including relay for controlling an external alarm. Audible alarms are optional. From $1095 to $2995. **Acopian**, Easton, PA. (800) 523-9478.
Circle No. 426

150W power supply meets the European EMC directive. The PFC150 Series power supply is a power-factor-corrected, switched-mode power supply that deals with all aspects of the EMC directive and meets the EN60555-2 standard. The 100-kHz MOSFET design includes EMI filtering to EN55022 curve B, one to five outputs, overload and overvoltage protection, and a single-range worldwide 90- to 264V-ac input. The supply comes in a 2.4×4.5×8.3-in. package. From $210 (100). **Unipower Corp**, Coral Springs, FL. (305) 346-2242. **Circle No. 427**

270V military dc/dc converter has nearly 50W/in.³ power density. The SM200S-270 dc/dc converter family accepts 28 or 270V dc and provides a single output of 2, 3.3, 5, 5.2, 12, 15, 24, or 28V dc. The 4.2×2.4×0.5-in. converter provides peak rated power from –55 to +100°C. Line and load regulation are typically better than 0.2%, and remote sensing compensates for a drop of up to 0.5V in the leads. From $600 (OEM qty). **Abbott Electronics Inc**, Los Angeles, CA. (310) 202-8820.
Circle No. 428

350W power supplies are hot-swappable. HP Series enclosed, hot-swappable power supplies suit RAID-based systems. The 5×2×10.5-in. supplies are available in models with one to four outputs from 2 to 28V dc. Features include protection from input surge, overvoltage, and overtemperature. The supplies also provide current limiting and current sharing with N+1 redundancy. You can configure all models with or without an auxiliary dc fan. From $375 (small qty). **Omega Power Systems Inc**, Chatsworth, CA. (818) 727-2216. **Circle No. 429**

DC/DC converters offer a 20 to 72V input range and efficiencies to 80%. The FM series converters are housed in a 2.5×3×0.5- or 2.6×4-×0.54-in. package, including flange mounting for rugged environments. The case also has pins for pc-board mounting and six-sided shielding. $65 (OEM qty). **Semiconductor Circuits Inc**, Windham, NH. (603) 893-2330.
Circle No. 430



Output modules for VXIbus power supplies offer current sharing and redundant operation. VX Series supplies with "enhanced-output" options offer current sharing for parallel or N+1 redundant operation, dc-output-good signals, remote inhibit, and VME/VXI power-fail monitor. The series is available in power ratings of 500, 750, 1000, and 1500W. Each model provides seven VXIbus outputs. A typical 750W supply with enhanced outputs costs $0.90/watt (OEM qty). **Deltron Inc**, North Wales, PA. (215) 699-9261.
Circle No. 431

5-kVA-rated UPS provides 21 minutes of backup at full load, 60 minutes at half load. OnGuard Elite 5000 is a dual-conversion, on-line UPS (uninterruptible power source) that provides pure sinewave power to all attached equipment. The unit performs as a precision power regulator and conditioner, protecting sensitive electronic equipment from damaging frequency and voltage fluctuations. The UPS has

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Now, from the innovator in integrated switching regulators, comes a new series of high-performance 5V to 3.3V, 3A and 8A single in-line products. The new Power Trends PT63/65 series lets you easily solve the problem of integrating 3.3V logic into existing 5V systems, ***without redesigning your power supply.***

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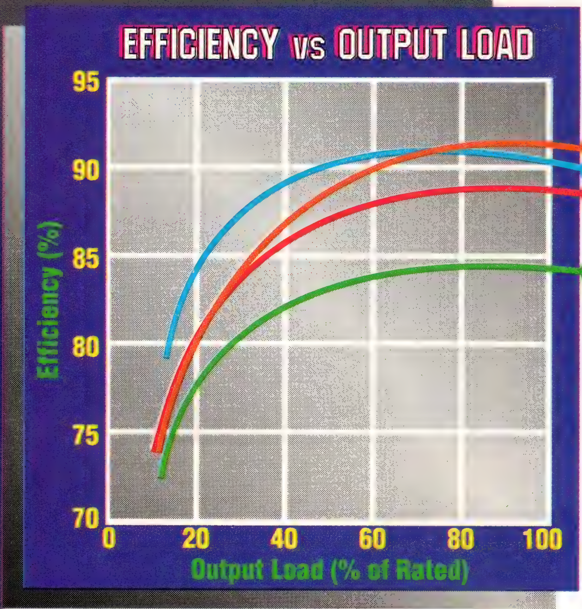
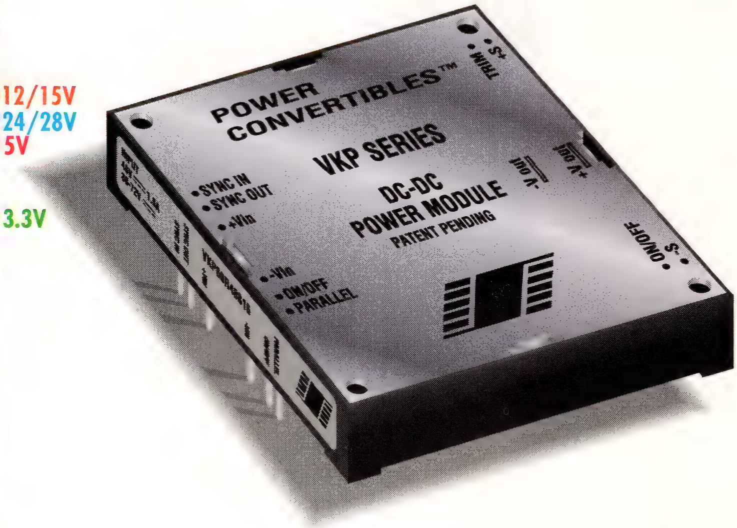
CIRCLE NO. 124

91% EFFICIENT 60 WATTS

DC/ DC CONVERTER





We've broken the 91% efficiency barrier in a standard "half-pack", 2.3" x 2.4" x 0.45" package with our new VKP Series DC/DC converters.

Innovative circuit design utilizing surface mount technology enables the VKP Series to dissipate 60% less power (heat) than competition over the full load range.

Full functionality includes primary and secondary remote on/off, synchronization input/output, output voltage adjust, remote sense and parallel/load sharing capability.

Currently is offered in a 36-72 volt input range, the VKP series is ideal for telecommunications, distributed power architectures and workstations.

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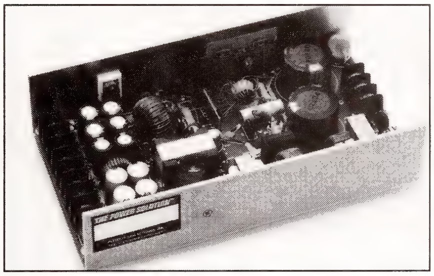
CIRCLE NO. 32

microprocessor-based circuitry and an RS-232C communication link that monitors system operation, operation history, and alarm message logging. The UL-listed units are FCC Class A rated and IEEE 587/ANSI C62.41 compliant. $9421. **Clary Corp**, Monrovia, CA. (818) 359-4486. **Circle No. 432**

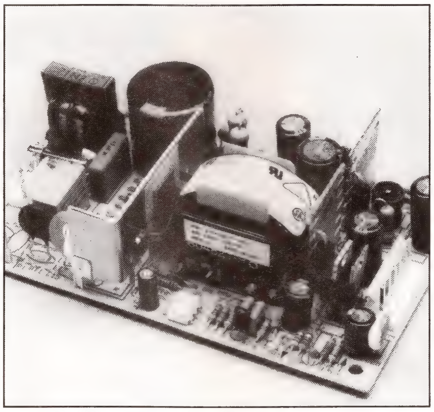
285W ac/dc supply is hot swappable in an N+1 current-sharing configuration. The 151 Series supply accepts a 90 to 264V ac input and provides 5V dc at 35A and 12V dc at 9A. The supply includes an output-good signal and remote on/off signals. Supply dimensions are 13×6×2.5 in. **Conversion Equipment Corp**, Orange, CA. (714) 637-2970. **Circle No. 433**

50W-dc supplies now have dc-input option. The universal-input, 50W Easymod multiple-output switching power supplies accept dc input for telecommunication and uninterruptible-power-supply applications. The AD 50 series models are 3×5×1.5 in. and are available with input ranges of 9 to 20, 18 to 36, 36 to 72, 18 to 72, and 120 to 130V dc. The supplies are available with one to four outputs from 5 to 56V dc. Single-output models start at $75 (100), and multiple-output models start at $80 (100). **Power Solutions Inc**, Pompano Beach, FL. (305) 943-4110. **Circle No. 434**



300W supplies for telecommunications accept ac and dc inputs. The AG series 250W (300W peak) EASY-MOD switching power-supply family has an autoranging 85 to 132/170 to 264V ac input. A dc-input version in the same package is available with input ranges of 9 to 20V, 18 to 36V, and 36 to 72V. The units are housed in a 8×4.5×2-in. package and have one to four outputs from ±2 to ±56V dc. The ac models, from $209; dc models, from $272 (OEM qty). **Power Solutions Inc**, Pompano Beach, FL. (305) 943-4110. **Circle No. 435**

Autoranging 200W ac/dc power supplies cost $90 in OEM qty. The PU200 Series switching power supplies have a 90 to 130/180 to 264V ac autoranging input, typical efficiency of 70%, a power-fail-detect signal, and a hold-up time of 20 msec minimum. An integral EMI filter limits conducted emissions to VDE Level B and FCC Class B. Single- and multiple-output models are available in a 9×5×2.55-in. package. Single-piece price starts at <$200. **International Power Sources Inc**, Ashland, MA. (508) 881-7434. **Circle No. 436**



Low-cost, open-frame power supplies meet VDE B EMI limits. The NAN family of 25W ($25 to $28 (OEM qty)) and 40W ($28 to $31 (OEM qty)) ac/dc power supplies have low-noise designs to meet FCC and VDE 0971 level B line-conducted noise limits. Single-, dual-, and triple-output models are available with efficiencies to 70%. The supplies operate from 90 to 264V ac and have a holdup time of 10 msec at 110V ac. The supply dimensions are 5×3×1.2 in. Peak-to-peak ripple is 1% of nominal output voltage on each output. Total regulation is ±3% for the main output and ±5% for auxiliary outputs. **Computer Products Inc**, South Boston, MA. (617) 268-1170. **Circle No. 437**

1.25- to 3-kVA UPS available in rackmount militarized version. The Battlefield Power series UPSs measure 3.5 in. high; you can mount them in 19-in. rack or tower configurations. The units meet shock and vibration requirements of MIL-STD-810E and all quality system requirements of MIL-STD-45208. MTBF is 150,000 hours. Input voltages are 80 to 280V ac and, optionally, 28V dc. The pure-sine-wave output is regulated to ±2% in frequency and voltage. Power factor correction, which meets IEC 555-2, is standard. From $2715. **Technipower Inc**, Danbury, CT. (203) 748-7001. **Circle No. 438**

UPSs with external battery packs provide unlimited backup time. By using external battery packs, you can extend backup time of the PowerRite EB Series of UPSs. The battery packs have their own internal charger for fast recharge, regardless of the number of external battery packs you use. The batteries recharge to 90% capacity in four hours. The 1500-VA unit costs $1669; the 2000-VA unit costs $1779. **Deltec Electronics Corp**, San Diego, CA. (619) 291-4211. **Circle No. 439**

50W dc/dc converter provides up to 500V output. The H50 Series converters offer input ranges of 9 to 36V and 20 to 60V. You can specify outputs from 50 to 500V. The 100-kHz switching frequency results in typical efficiencies of 90%. The modules are housed in a copper case measuring 2.56×4.56×0.83 in. $135 (100). **Orion Industries Inc**, Windham, NH. (603) 894-4242. **Circle No. 440**

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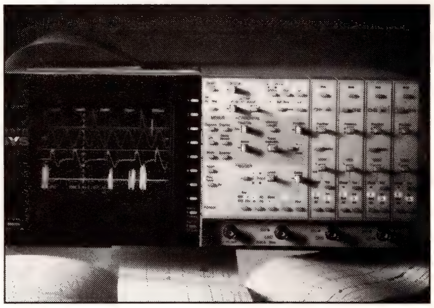
System upgrade improves board-test productivity. An SCO-Unix PC replacement for the company's GR228X Board Test System replaces an existing VMS-based environment. According to the company, the change improves system productivity by up to 50%. $20,000 for subscribers to the GenRad software-support program and $26,000 for nonsubscribers. **GenRad Inc**, Concord, MA. (508) 369-4400.
Circle No. 382

Rocky Mountain Basic now runs under Windows. HTBasic for Windows lets you port HP Basic code to Windows from HP workstations (and vice versa). The software runs under Windows 95 (Chicago) or Windows 3.1 and is implemented in 32-bit code. Programs are file compatible with DOS PC, DOS 386/486, HP 7800, and Sun SPARCstation versions of the company's Basic. $925. **TransEra Corp**, Orem, UT. (801) 224-6550. **Circle No. 383**

Enhancements to network-monitoring and -diagnostic system. The IDMS-3000 manager ($2500) features a user interface that lets you select the types of views you prefer, such as viewing statistics from multiple LAN segments simultaneously. The internetwork delay and reachability application ($2500) measures network performance. Two probes periodically communicate with each other to compile a profile of the round-trip delay over some polling interval. If the measured delay is greater than a user-selected threshold, the system notifies the network manager. **Wandel & Goltermann Inc**, Morrisville, NC. (800) 277-7404.
Circle No. 384

Plain language calculation software runs under Windows. TK Solver for Windows lets you state numerical problems in plain language and then solves them. You don't have to rewrite equations to isolate unknown variables. No programming code is required. Introductory price, $199. **Universal Technical Systems Inc**, Rockford, IL. (815) 963-2220.
Circle No. 385

Test software for digital IC tester. Attest Software is providing its TDX-IDDQ test software for use with Alpine Image Systems' ScanFixture test system. The software is a fault simulator for CMOS circuits on which current measurement performs testing. The software computes short fault coverage for each applied vector, and selects vectors to achieve the desired coverage. From $5000. **Attest Software Inc**, Santa Clara, CA. (408) 982-0244.
Circle No. 386



150-MHz DSO includes chart recorder. The DataSys 760 uses a thermal printer to record waveforms on paper at 200 msec to 200 sec/division. The four-channel digital storage oscilloscope (DSO) with color display has a 100M-sample/sec sample rate and a 50,000-word memory for each channel. IEEE-488 and RS-423 interfaces are standard. From $10,490. **Gould Instrument Systems Inc**, Valley View, OH. (404) 328-7263. **Circle No. 387**

Data-acquisition boards scan 16 channels at 10-μsec/channel and 12-bit resolution. The DaqBoard/100A ($995) and DaqBoard/112A ($795) maintain the 10-μsec/channel scan rate when expanded to as many as 256 channels. You can program each channel for a different dynamically selectable gain. Dynamic gain selection lets you measure data from various signal sources without slowing the data-acquisition rate. The boards include two D/A channels, 16 digital input lines, 24 digital I/O lines, and (on the DaqBoard/100A) five independent 16-bit counters. The boards come with DOS drivers for Quick Basic, C, and Pascal; Windows drivers for Visual Basic and C++; and Visual Basic extension (VBX) custom controls. The included DacView2 Windows application lets you configure the board to acquire data. **IOtech Inc**, Cleveland, OH. (216) 439-4091. **Circle No. 388**

MICRO-CAP IV 3.0
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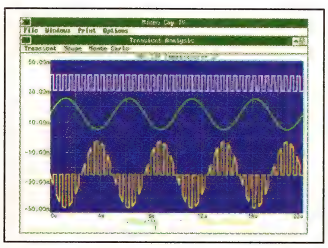

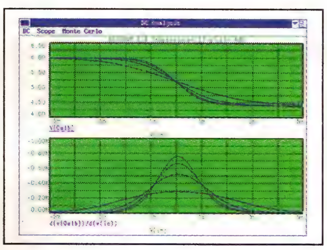

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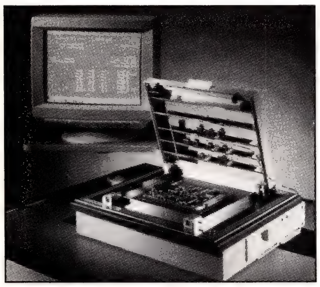
CIRCLE NO. 144

Notebook-PC-based portable data-acquisition system for thermocouple and voltage measurements. The TempBook/66 has a 12-bit 100k-sample/sec converter and accepts either eight differential or 16 single-ended analog input channels. The system also has cold-junction compensation and offset-correction for accurate and stable temperature measurements. I/O includes eight digital inputs, eight digital outputs, a 16-bit counter/timer, and TTL trigger input. A programmable gain amplifier lets you select channel gain individually. The unit measures 8.5×11×1$^3/_8$ in. and can connect to a PC via a standard parallel port, an enhanced parallel port (EPP), or an optional PCMCIA adapter. It operates from ac, dc, or batteries. $995. **IOtech Inc**, Cleveland, OH. (216) 439-4091. **Circle No. 442**



Vectorless test system finds assembly faults on SMT boards. The WaveScan vectorless test system finds and diagnoses assembly-process faults, such as digital and mixed-signal opens without traditional in-circuit patterns or vectors. Using hardware and software on the company's Z1800-series board testers, the product checks for continuity between a device lead and a board using RF stimulus and measurement. The RF technique detects manufacturing faults on VLSI devices, including opens, bond-wire opens, blown buffers, misoriented devices, and hairline solder cracks. It also finds opens on power or ground pins on devices having one power or ground pin. Retrofit systems cost $22,000. **Teradyne Inc**, Boston, MA. (617) 482-2700. **Circle No. 443**

Low-cost data-acquisition software. PC-SCOPE 2.0 is a $39 software package that works with the company's low-cost data-acquisition boards for PCs. An 8-bit 400k-sample/sec data-acquisition board costs from $89. **Bsoft Software Inc**, Columbus, OH. (614) 491-0832. **Circle No. 444**

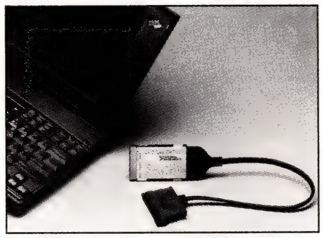
Neural-network software runs under Windows. BrainMaker Professional v4.0 has more than 30 new features to simplify and to improve network analysis and training. The software has full spreadsheet capability for data entry, editing, and formula entry. It reads and writes Excel or Lotus 1-2-3 files. New training algorithms train in one pass. A range of new analysis tools helps you check training and network performance. $795. **California Scientific Software**, Nevada City, CA. (916) 478- 9040. **Circle No. 445**

Antialiasing filter module multiplexes up to eight channels. The SCXI-1141 eight-channel elliptical lowpass filter module is compatible with the company's SCXI data-acquisition (DAQ) and signal-conditioning product line. Each channel features a differential instrumentation amplifier with software-programmable gains and input autozeroing. Each channel also has an eighth-order elliptical lowpass filter that provides a sharp 135-dB/octave roll-off, suiting the filter for antialiasing applications. An external-clock input and output on the module lets you set the filter cutoff frequency with an external clock in tracking filter applications. $1795. **National Instruments**, Austin, TX. (512) 794-0100. **Circle No. 446**

Filter-design-software add-on to graphical data-analysis software lets you test filters with data. The DADiSP/Filters 3.0 digital-filter-design software is a menu-driven, digital-filtering module that provides full FIR and IIR filtering capabilities on top of the DADiSP Worksheet. The new version increases the number of functions available to design, analyze, process, and display digital filters. You can use the filters on measurements transferred from a digital oscilloscope, spectrum analyzer, and other devices. $495 (for PCs); $995 (for workstations). **DSP Development Corp**, Cambridge, MA. (617) 577-1133. **Circle No. 447**

Control remote instruments via modem. The ModemNOW! communications tool kit lets you control RS-232C or IEEE-488 instruments directly from a Labview program. The library of virtual instruments lets you configure a modem, dial a remote site, establish communications, and send or receive data. After connecting to the remote site, you control instruments as if they were connected locally. $199. **Microsys Technologies Inc**, Toronto, ON, Canada. (416) 538-9443. **Circle No. 448**

500-MHz DSO family enhanced with more memory and processing power. The 9350 DSO family is now available in an A version. Base-version 9350/9354A has memory for 50k records/channel. The AM version has increased memory from 100k to 250k records/channel; the AL version offers 2M records of memory per channel. The 9354T and 9354TM include a 3.5-in. floppy and a math pack that performs FFTs, integration, differentiation, logarithms, exponents, absolute value, square, square root, six selectable digital filters, and averaging of 1M waveforms. From $9990 (for the two-channel, 1G-sample/sec 9350A) to $24,490 (for the four-channel, 2 G-sample/sec 9354AL). **LeCroy Corp**, Chestnut Ridge, NY. (914) 425-2000. **Circle No. 449**



PCMCIA card provides 24 digital I/O lines. The DAQ-Card-DIO-24 type II PCMCIA features a 24-bit programmable peripheral interface and data-transfer rates up to 250 kbytes/sec. The card connects notebook computers to peripherals with parallel digital I/O and comes with NI-DAQ and DAQWare software. $195. **National Instruments**, Austin, TX. (512) 794-0100. **Circle No. 450**

Scientific graphing software for Windows provides 2- and 3-D plotting. SigmaPlot Version 2.0 for Windows provides a rigorous implementation of 2-D contour plots. The software automatically labels contour lines as it generates them. $495. The SigmaPlot Graph Library accessory ($99) provides more than 150 publication-quality graph types to use as templates for your own data. **Jandel Scientific Software**, San Rafael, CA. (415) 453-6700 **Circle No. 451**

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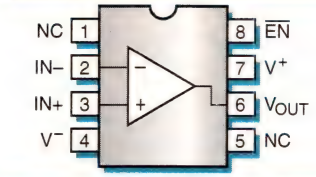

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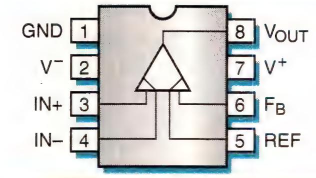

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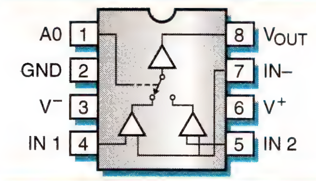

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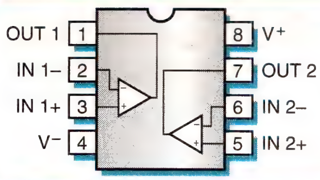

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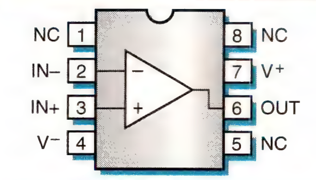

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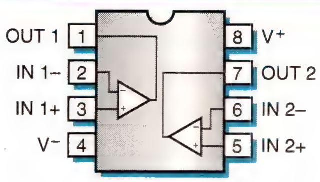

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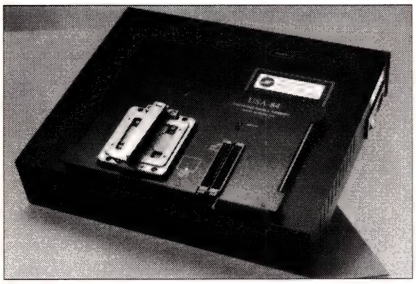

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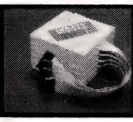

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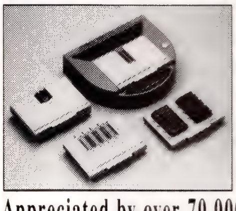

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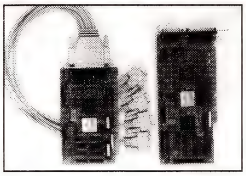

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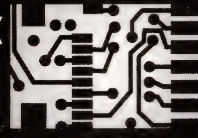

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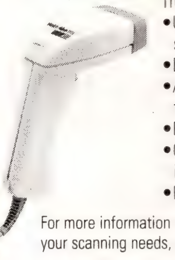

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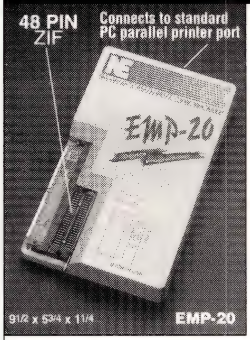

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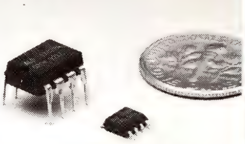

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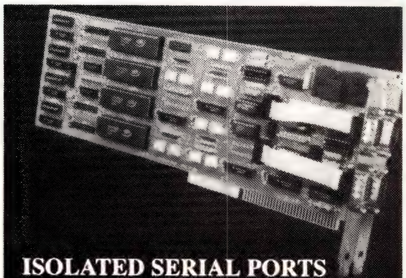

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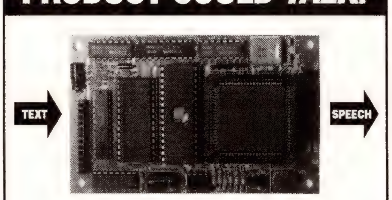

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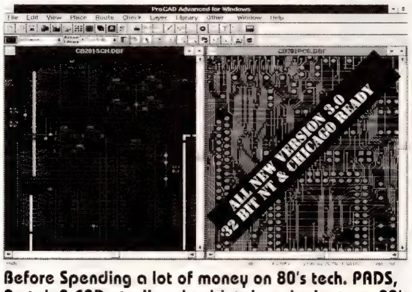

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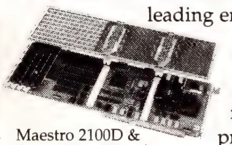

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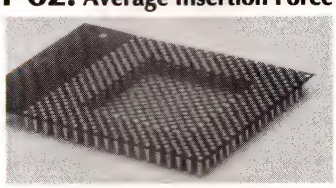

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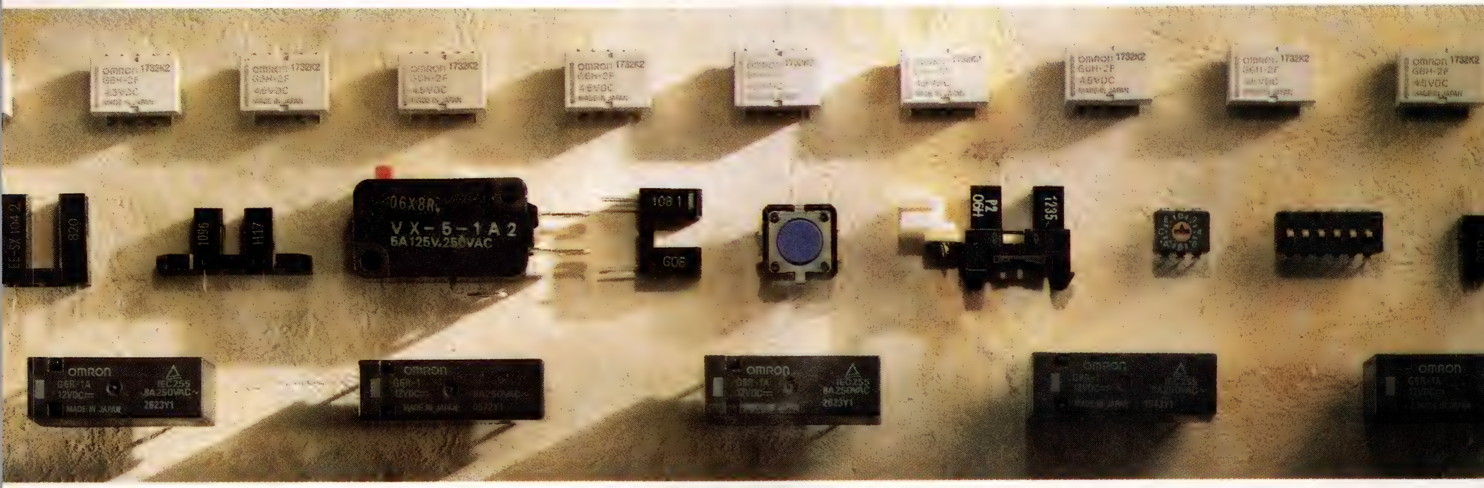

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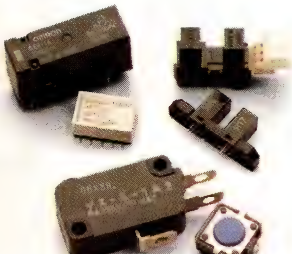

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Simulation in fuzzy-controller design

In my seven-year career as a basketball player—seventh grade through freshman year in college—the most fun I had was during the last eight weeks of the last year. The freshman coach suggested it would be good for me to get varsity experience and invited me to join the "Red Team," those players who studied films of opposing teams and attempted to emulate those teams in practice.

This was great fun, working hard with the rest of the Red Team to put together both the offenses and defenses of the other PAC-8 teams. Of these teams we tried to be, the only one I clearly remember is UCLA. That was Lew Alcindor's (now Kareem Abdul-Jabbar's) sophomore year, and with him as center, the Bruins went on to win the NCAA championship that year, and the next two years as well.

What does this have to do with fuzzy logic—beyond our Red Team being in the set of UCLA-like basketball teams with degree of membership less than or equal to 0.01? The stretch is actually not that great. In emulating other teams, the Red Team was a simulation. Varsity could not practice against the actual teams they would face, but they needed to prepare. We Red Team members did our best to simulate the other teams, and, overall, I believe we helped.

Simulation also plays an important role when designing fuzzy systems, especially fuzzy controllers. For a number of reasons, a designer often cannot connect the controller being developed directly to the controlled system until late in the development process. In early design stages, he or she must instead use a simulation environment. Just as the varsity coach used the Red Team's simulation of Stanford's opponents to design and refine plays, options, and defenses, the fuzzy-system designer uses a simulation of the controlled system to design and tune the fuzzy controller.

There is another similarity. My Red Team was a poor simulation of the UCLA Bruins. Similarly, in system design, a good simulation model is often difficult to create; recall that fuzzy systems are often the best solution when an analytic model of the controlled system is unavailable. The easy justification, the one we used as the Red Team, is that a poorly representative model is better than no model at all.

In fuzzy-system design, there is deeper, more significant justification. Because of the robustness of fuzzy systems, their insensitivity to variations in the parameters of the systems they control, a poor-quality model can be extremely helpful in the design. Designers have noticed that they often do not need to perform final tuning of fuzzy parameters when interacting with the actual target system, even when the simulation model used during design inadequately represents the system it is modeling. This is an often overlooked feature of fuzzy systems.

There is a purpose for this lengthy introduction. This month we will discuss the use of a simulator in designing the rulebase of a fuzzy system. Our model is simple, and the simulation therefore accurate. The model is of the series RLC circuit introduced last time (*EDN*, January 5, 1994, pg 167).

Recall that we are designing a fuzzy PD+I controller that charges a 100-μF capacitor through a 10-mH inductor (**Fig 1**). We'll design the PD part of the system first, concentrating on meeting rise time and overshoot requirements, less than 1 msec and less than 5%, respectively. Once satisfied with the PD response, we'll implement the I (integral) component separately, using it to minimize steady-state error.

We start with the membership functions. Defining them is the simplest part of the design. As discussed last time, we will work with normalized domains, deferring dealing with real-world ranges until later.

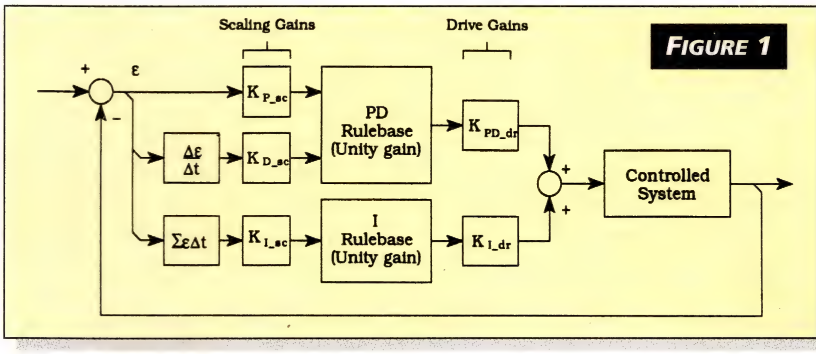
For both the error value, *error*, (the P input) and its derivative, *error_dot*, (the D input), we define seven fuzzy values, and therefore seven membership functions (**Fig 2a**). The number seven is somewhat arbitrary, although most simple to moderately complex systems use between three and seven fuzzy values for each input.

For function shapes, we choose broader membership functions for the regions removed from zero where we want coarse control, and narrower functions for the regions close to zero where we need fine control. Although any appropriate function representation is possible, we'll use triangles and trapezoids, which are easier to represent and to work with.

The PD output is the V_{IN} applied to the RLC circuit. Again, with normalized domain, we will use seven singletons as the possible actions, spaced evenly between ±1, inclusive (**Fig 2b**). A singleton is a single, scalar output value. It is not a fuzzy set, represented with a membership function, but is rather a single, crisp value. In a future column, we will discuss types of defuzzification and compare fuzzy output sets combined and defuzzified using center of mass to singletons combined using a weighted average. The two achieve quite similar results, and in control, where execution speed is important, I will most often use singletons.

If creating membership functions is the easiest design step, identifying rules is the most complicated (**Fig 3**). We will now start using the simulator. The "design" process consists of repeatedly resetting the simulator to its initial conditions and

FIGURE 1

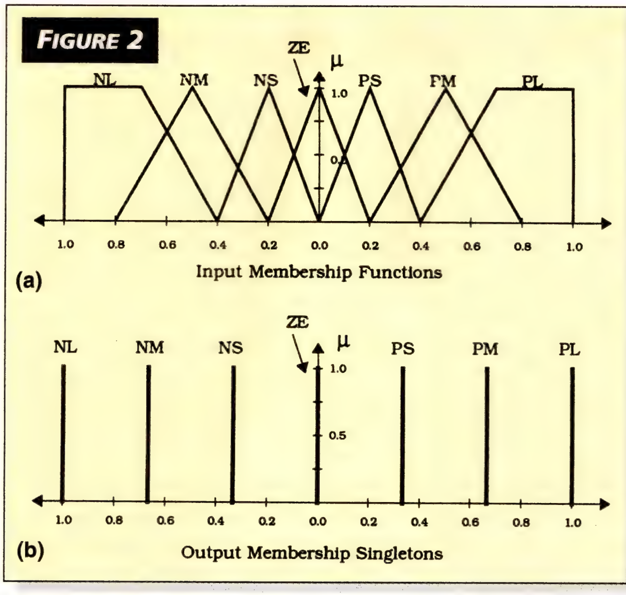


A fuzzy PD+I controller charges a 100-μF capacitor through a 10-mH inductor.

PHOTOGRAPHY / LIANE ENKELIS

single-stepping through a commanded input voltage step. Each time the system enters a region in the input space with an as-yet-undefined action, the designer determines an appropriate output action, inserts this into the rule specified by the given input space, and single-steps the simulator into the region. If the selected action is correct, system operation will be as desired. If not, the designer specifies a different action and restarts the simulation. The designer repeats this sequence of restarting, single-stepping, and testing numerous times until he or she has defined the entire rulebase.

Let's see how this works. From experience, we know that bang-bang control can effectively move a system close to its setpoint, after which some form of continuous control achieves and maintains the setpoint. This is a traditional method of using highly undamped control far from the setpoint and allowing it to give way to a damped control near the setpoint. This is the approach we shall take with the fuzzy controller.



The plot in (a) shows the input membership functions used for both the P and D inputs. Both domains range between ±1.0, with appropriate scaling performed by scaling gains. Input membership functions are standard, with functions nearer to zero being somewhat more narrow than functions farther from zero. The plot in (b) shows the output singletons used for the PD drive, V_{IN}.

Fig 3a shows the desired operation of the system. When the actual and commanded capacitor values are equal, both *error* and *error_dot* are zero—the system resides in cell A. If the command is for a positive voltage step, the system jumps horizontally to B. As the capacitor starts to charge, the derivative goes negative until *error* is PL (Positive_Large) and *error_dot* is NL (Negative_Large)—the upper right corner of the matrix.

The capacitor continues to charge, and as *error* becomes smaller, the system enters region C. If the designer has correctly assigned rule actions, the system will quickly spiral through regions C and D and back toward cell A. This is the setpoint.

The heavy black line below region D is a boundary the response cannot pass, because the unshaded cells in **Fig 3a** must be the mirror image of the shaded cells to respond to a negative step command; that is, they must have identical amplitude but opposite polarity actions. If the system response crosses the black line during the last stages of a positive step, it will act as if it were in the middle stages of a negative step response.

Fig 3b shows the regions in the order that rules are assigned. Assume the system is at rest with the capacitor fully discharged and with no current flowing—it is in cell 1 at the center of the matrix where *error* and *error_dot* are both ZE (zero). Using the simulator in single-step mode, the designer commands the system to step to 5V. The system jumps laterally into region 2, to the cell "*error* is PL AND *error_dot* is ZE."

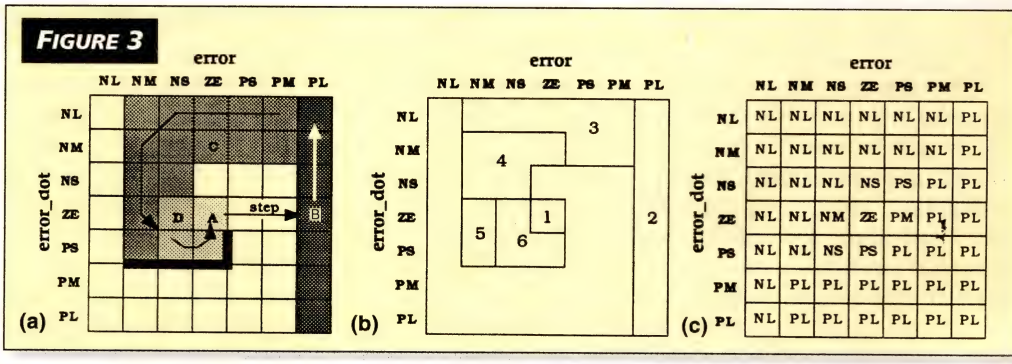
We want a maximum positive output where there is a large, positive error; this is the first "bang" of the bang-bang controller. We therefore assign PL (Positive_Large) as the action for all cells in region 2. For example, the rule for the center cell in the column is

IF *error* is PL AND *error_dot* is ZE THEN V_{IN} is PL;

Using the simulator, we check to see if the response is what we expected. It is. In response to the large positive drive, the simulated capacitor starts to charge, and after several Δt increments, the derivative term decreases from zero to Negative_Large (NL). The system is now in the upper right cell in the matrix.

As the error decreases further, the system enters the second region of the phase plane, the first cell being where "*error* is PM AND *error_dot* is NL." We want this region, labeled 3 in **Fig 3b**, to provide the second bang—to put on the brakes. We therefore set all cells in this region to NL.

As we continue to step the simulator, the response continues toward the left and across the top of the rule matrix, where *error* is decreasing but *error_dot* remains maximum. Even as it moves into and through regions 4 and 5 of **Fig 3b**, we continue to require the large



These three matrices are of the rulebase that is used for the PD component of the controller. The matrix in (a) shows the desired control actions. The figure (b) shows the sequence taken to design the rulebase, and (c) shows the final set of rules.

negative output, NL. Only as the response moves into region 6 do we terminate bang-bang control and allow less than maximum outputs to dampen the system in toward the setpoint. By continuing to step the simulator through its sequence, the rules for the three cells in Region 6 become

IF *error* is NS AND *error_dot* is ZE THEN V_{IN} is NM;
IF *error* is NS AND *error_dot* is PS THEN V_{IN} is NS;
IF *error* is ZE AND *error_dot* is PS THEN V_{IN} is PS;

Fig 3c shows the completed rule matrix, with the actions for a negative commanded step added as well. Note that the rulebase shown in **Fig 3c** is for the full PD+I implementation. For the PD-only system, I used a rule action of PL (Positive_Large) for the rule with condition error is ZE (zero) and error_dot is PS (Positive_Small), intending to minimize as much as possible the offset error. When we add integral control, we can reduce the PL action to PS.

With the exception of this single rule (and its negative step counterpart), the rulebase existed in its final form after the first design cut. The total rule design process took approximately two hours and involved single-stepping and running numerous simulations while identifying and modifying rules for the various cells. The membership functions did not change from their initial shapes and positions.

However, I definitely "played" with the scaling gains as part of the tuning process. As shown in **Fig 1**, the PD part of the controller has three gains associated with it: scaling gains for the P and D components, and a drive gain for the combined PD output. We first set scaling gains to allow maximum error values to fully exercise the normalized input domains, and we'll subsequently modify them as part of system tuning.

Setting the initial gain for the P term is straightforward. Recall that we normalize values into a ±1.0 range. The maximum possible error for the P term is 5V, and we therefore use a scaling gain of 0.2. To set the D scaling gain, we could calculate the maximum anticipated charging current and thereby the maximum anticipated dV/dt. However, it is simpler to use the simulator to apply full drive to the RLC circuit and watch the capacitor charge to one-half the maximum step size. Doing so, we observe a maximum ΔV of approximately 0.4V per sample interval Δt and therefore set the initial D scaling gain to 2.5. Incidentally, in the simulation, we multiply $\Delta V/\Delta t$ by Δt to have the derivative input in terms of volts.

We also select the PD drive gain empirically, with an initial value of 20 to provide sufficient drive in the first half of the step response to keep the drive voltage to the RLC circuit saturated. A maximum rulebase output of +1 would result in an applied V_{IN} of 20V, limited by the physical system to +15V.

In the next column, we'll complete the design by building the I (integral) leg of the controller.

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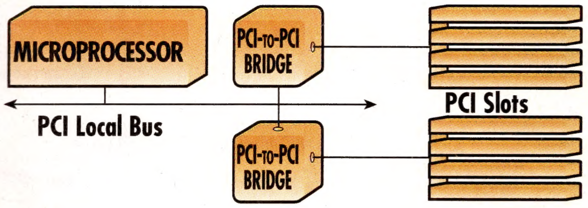

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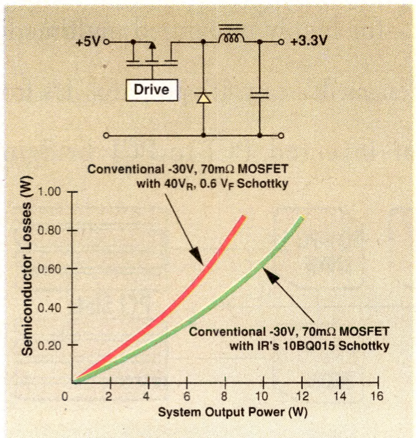

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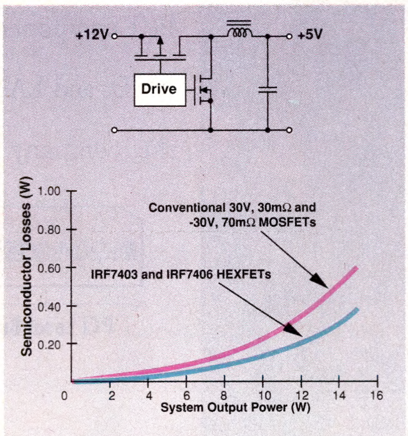

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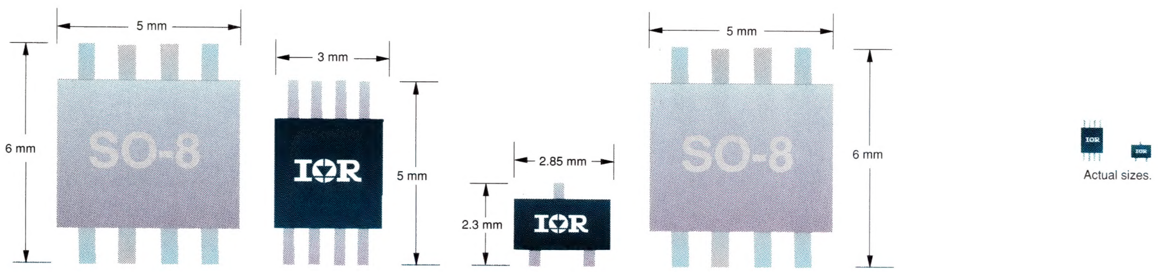

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P-Chan. (2)	IRF7504 IRF7506	-20 -30	0.27 0.27
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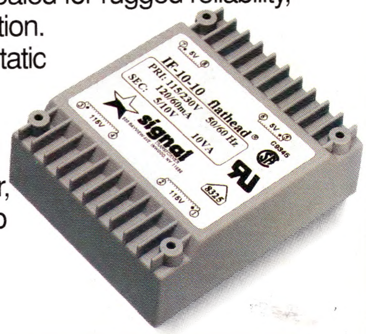

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- VDE certified to IEC 950

International Flathead™ (IF)Series

VA (Size)	L	W	H	Wgt
2	2.09″ 53.0mm	1.73″ 44.0mm	0.69″ 17.6mm	4.6 oz 0.13 kg
4	2.09″ 53.0mm	1.73″ 44.0mm	0.77″ 19.6mm	5.4 oz 0.15 kg
6	2.09″ 53.0mm	1.73″ 44.0mm	0.89″ 22.6mm	6.9 oz. 0.20 kg
10	2.66″ 67.6mm	2.24″ 57.0mm	0.89″ 22.6mm	10.3 oz 0.29 kg
14	2.66″ 67.6mm	2.24″ 57.0mm	0.96″ 24.3mm	11.9 oz 0.34 kg
18	2.66″ 67.6mm	2.24″ 57.0mm	1.09″ 27.6mm	14.1 oz 0.40 kg
24	2.68″ 68.0mm	2.26″ 57.5mm	1.23″ 31.3mm	16.5 oz 0.47 kg
30	2.68″ 68.0mm	2.26″ 57.5mm	1.39″ 35.3mm	19.7 oz 0.58 kg

Output voltages available from 5V to 230V

Custom versions also available

BUY DIRECT: (516) 239-5777

FAX REQUIREMENTS TO: (516) 239-7208

PRONTO: 24 hr. off-the-shelf shipment

Signal Transformer

CIRCLE NO. 138